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Geometric Phased Beam Diver Held Sonar Final Report

R. L. Tutwiler, C. W. Allen, W. J. Hughes

Technical Memorandum

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Abstract: A design for an underwater acoustic imaging system that would be portable enough to be operated by a diver was developed utilizing the geometric phased beam or "doily" array concept. The "doily" array design provides multiple beamsteering capability while drastically reducing the number of elements required. The system would operate in the 1 to 6 MHz frequency range and only require 1808 channels. This report documents the state of the design at the end of the program.

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Name and Title of Certifying Official: Dr. E. G. Liszka
Dr. E. G. Liszka, Director

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1.0 INTRODUCTION

The objective of the Diver Held Sonar program funded under the Office of Naval Research Grant N00174-98-1-0032 was to develop, fabricate, and test a prototype diver hand-held sonar system that could image mine-like objects at ranges from 3 to 5 meters. Due to the loss of funding, the program was not completed, but various components of the system were developed to different levels of completion. A conceptual sketch of the system is shown in Figure 1. The components of the system are:

- Acoustic array
- Array interconnect board
- Preamplifiers
- Transmitter
- Array analog phase and summing electronics
- Analog-to-digital conversion (A/D)
- Horizontal beamformer
- FFT processor
- Display
- Mechanical packaging

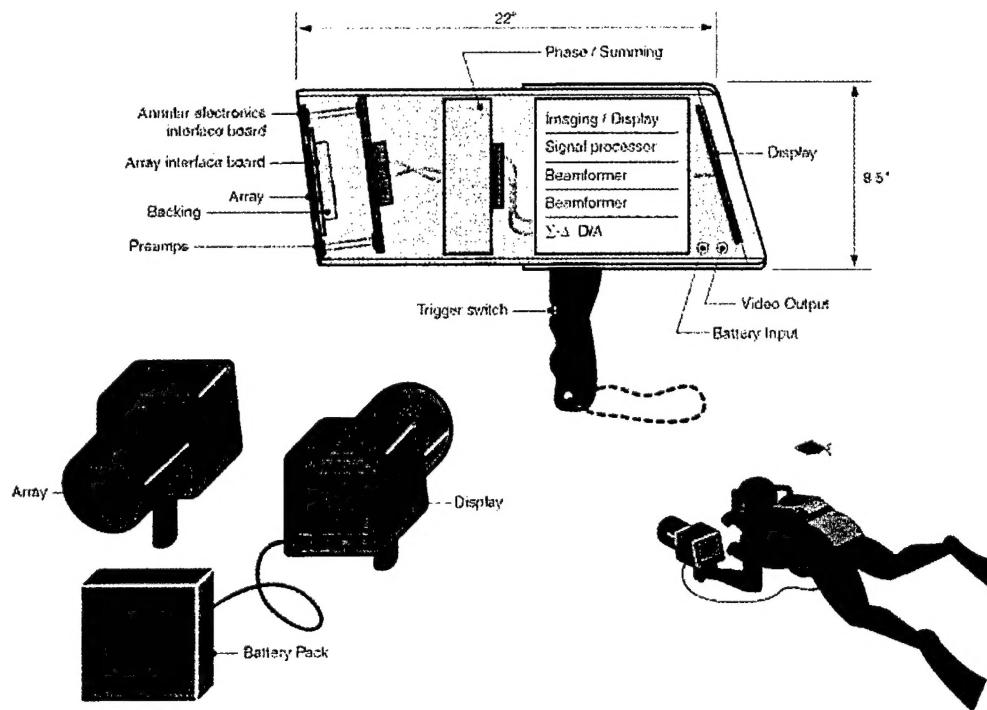


Figure 1. Geometric Phased Beam "Doily" Diver Held Sonar Concept

One of the main features of this sonar design is the acoustic array, which implements an ARL Penn State patented (U.S. patent no. 6,108,275) geometric phased beam or "doily" technique for forming and steering beams. The "doily" array uses the physical location of the elements along with discrete phase shading in multiples of 90° to steer the beams as a function of frequency. This method drastically reduces the number of elements required from about 160,000 to a more realistic 1800. In this application, about 450 vertical staves are formed to form horizontal beams.

The “doily” method, which only requires four channels per stave, is used to form the vertical beams. The system operates in a frequency band from 1 to 6 MHz.

The actual array itself would consist of 1-3 PZT composite which would be divided into individual elements by dicing the electrodes. These elements would be connected together using an interconnect board which would also route the element groups (channels) to the T/R board. The array is driven with the transmit electronics to form vertical beams to match the receive beams. The receive signals are routed through the preamplifiers and the phase shift electronics where the required 90° phase shading would be applied to various channels and then summed together (this process for each stave is shown in Figure 2 and is explained in more detail in section 2.1). The analog signals are then converted into digital signals and then formed into horizontal beams using a conventional beamformer. The Fourier transform is taken of the resultant beams to form the “doily” vertical beams since the steer angle is a function of frequency. The resultant 2D image is then displayed on a screen. All of these components would then be packaged to be small enough for a diver to handle easily.

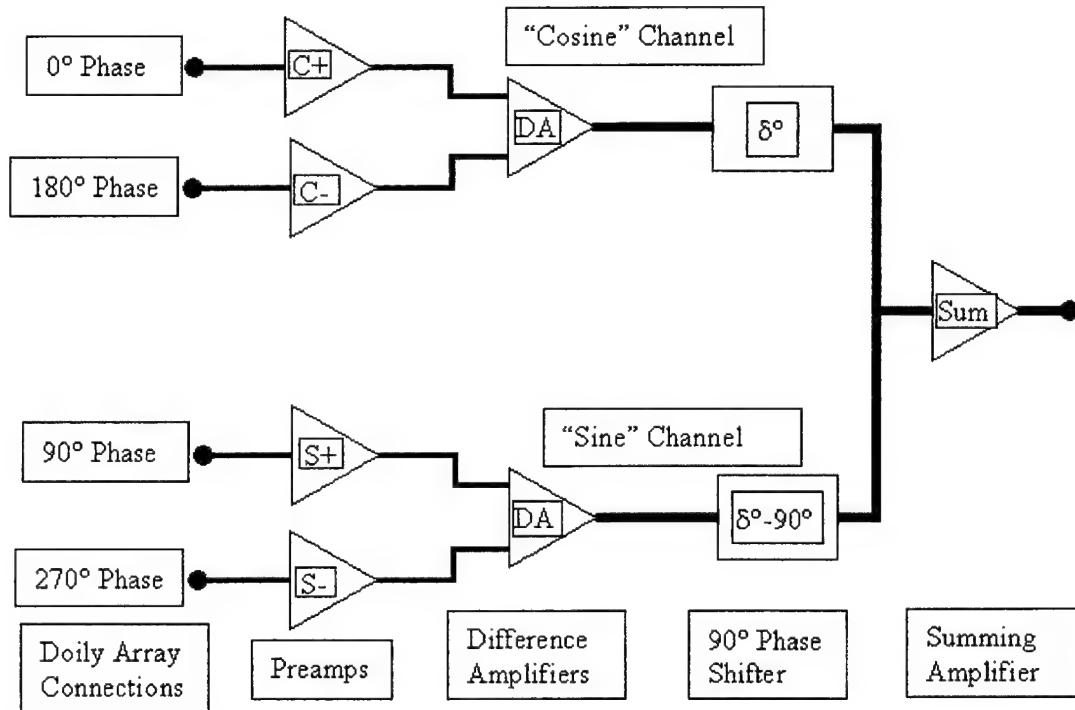


Figure 2. Four Channel 1D Doily

2.0 SYSTEM OVERVIEW

As mentioned earlier, the system consists of the Doily Array, Transmitter and the Receiver.

2.1 Doily Array

For acoustic communications, particularly in underwater acoustics, and particularly when the position of source or receiver is fixed, it is desirable to tilt the direction of maximum response of

the sum pattern of either a source or receiver array to bearing angles other than straight ahead. Furthermore, there may be instances when it is desirable to tilt the null of a difference pattern. Tilted patterns are conventionally formed by introducing time delays or phase shifts into the outputs of the individual elements of the array so that this added time delay or phase shift negates the geometric time delay or phase shift associated with the positioning of the elements relative to a planar wave-front propagating at the desired angle of maximum response. The individual element outputs then combine constructively at this new angle in the case of the sum pattern or destructively in the case of the difference pattern.^[1]

In this imaging system, a different method of achieving a tilted pattern from a symmetric shaped array without using numerous time delays or phase shifts is implemented. In fact, only one + or $- 90^\circ$ phase shift is required and different angles of tilt are achieved by varying the amplitudes of the outputs of the individual elements. The method is illustrated with theoretical calculations and experimental data for both a sum pattern and a difference pattern. Henceforth, the method is only discussed in the context of the receive mode of operation but it is evident that it will work equally well in the transmit mode. While this analysis and data pertain to a symmetric, uniformly spaced, line array configuration, the extension to other source configurations such as a symmetric but non-uniformly spaced line array or to a planar array is straightforward.

Analysis for the doily array is presented here. Consider a symmetric line array of point receivers each spaced distance d apart. To form a tilted pattern, an element on one side of the center must be phase delayed by Φ radians and the element symmetrically located on the opposite side of the center must be phase advanced by Φ radians. In practice, this is often accomplished by introducing progressive time delays into these outputs starting at one end of the array.^[2]

For an even numbered line array of $2n$ elements, the normalized directional response function for a tilted sum pattern can be written^[3]

$$P_{\Sigma}^E(\theta) = \{A_1 \cos(u - \phi) + A_2 \cos[3(u - \phi)] + \dots + A_n \cos[(2n-1)(u - \phi)]\}, \quad (1.1)$$

Where A_i are the weighting coefficients assigned to the element outputs to achieve, for example, some desired degree of the side lobe suppression (A_1 is the coefficient of each of the innermost pair of elements, etc.), $u = (kd \sin \theta) / 2$, $k = \omega / c$ is the acoustic wave number, ω is the circular frequency in radians/sec, c is the speed of sound in the medium, and θ is the angle of incidence relative to the normal to the array. To tilt the pattern to some angle θ_0 requires that the phase $\phi = (kd \sin \theta_0) / 2$. for a pattern tilted to the other side of the normal to the array, the sign of ϕ simply reverses. For an odd-numbered symmetric line array of $2n+1$ elements, the normalized, tilted-sum-pattern response function can be written

$$P_{\Sigma}^0(\theta) = 1/2B_0 + \{B_1 \cos[2(u - \phi)] + B_2 \cos[4(u - \phi)] + \dots + B_n \cos[2n(u - \phi)]\}, \quad (1.2)$$

where B_0 is the weighting coefficient of the central element, etc.

If Equations 1.1 and 1.2 are expanded using fundamental trigonometric identities, and the terms are regrouped, the following expressions are obtained:

$$P_{\Sigma}^E(\theta) = \{A'_1 \cos u + A'_2 \cos 3u + \dots + A'_n \cos[(2n-1)u]\} + \{A''_1 \sin u + A''_2 \sin 3u + \dots + A''_n \sin[(2n-1)u]\}, \quad (1.3)$$

where,

$$A'_1 = A_1 \cos \phi, A'_2 = A_2 \cos 3\phi, \text{etc.}, \quad (1.4)$$

$$A''_1 = A_1 \sin \phi, A''_2 = A_2 \sin 3\phi, \text{etc.}, \quad (1.5)$$

and

$$P_{\Sigma}^0(\theta) = \{1/2B_0 + B'_1 \cos 2u + B'_2 \cos 4u + \dots + B'_n \cos 2nu\} + \{B''_1 \sin 2u + B''_2 \sin 4u + \dots + B''_n \sin 2nu\}, \quad (1.6)$$

where,

$$B'_1 = B_1 \cos 2\phi, B'_2 = B_2 \cos 4\phi, \text{etc.}, \quad (1.7)$$

$$B''_1 = B_1 \sin 2\phi, B''_2 = B_2 \sin 4\phi, \text{etc.}, \quad (1.8)$$

Consider Equation 1.3. Because the first series in braces contains terms involving only the cosine of the variable u , it is the response functions of a certain phase-symmetric array, i.e., an array where elements symmetrically positioned with respect to the array center have the same amplitude and phase. This array is physically the same size as the original array of $2n$ elements but has new weighting coefficients given by Equation 1.4 note that these weighting coefficients are functions of the desired tilt angle θ_0 . The second series in braces contains terms involving only the sine of the variable u and is therefore the response function for a certain phase-antisymmetric array, i.e., an array where symmetrically positioned elements have the same amplitude but are 180° out of phase with each other. This array is also physically the same size as the original array but has still different weighting coefficients given by Equation 1.5.

Equation 1.3 indicates that the tilted pattern of Equation 1.1 can be synthesized by combining the output of the given array of $2n$ receivers connected as a phase-symmetric array with the amplitude weightings given in Equation 1.4 and the output of the same array connected as a phase-antisymmetric array with the amplitude weightings given in Equation 1.5. Note that the Equation 1.3 requires the two outputs to be combined in phase. However, since the output of an array when connected as a phase-antisymmetric array is inherently in phase-quadrature with its output when connected as a phase-symmetric array,^[4] an additional phase-quadrature factor must be introduced into one of these two outputs; the sign of this 90° phase shift determines the direction of tilt.

These same arguments are applicable to the tilted sum pattern response function of the odd numbered array given in Equation 1.6. In this case, the center element contributes only to the phase-symmetric array output. If, instead of adding the two components as indicated in Equation 1.3 or Equation 1.6, they are subtracted, a pattern tilted to the other side of the normal to the array is obtained.

This method can also be used to tilt a difference pattern. For an even or odd numbered line array, the normalized directional response function, for a tilted difference pattern is formally the same as Equation 1.1 or Equation 1.2, respectively, except that the cosine functions are everywhere replaced by sine functions. Of course, the values of the weighting coefficients A_i and B_i would probably be different than for the sum patterns and, for the odd array, the center element coefficient B_0 must equal zero. Expanding these difference pattern functions as before and regrouping the terms, one obtains

$$P_{\Delta}^E(\theta) = \{A'_1 \sin u + A'_2 \sin 3u + \dots + A'_n \sin[(2n-1)u]\} - \{A''_1 \cos u + A''_2 \cos 3u + \dots + A''_n \cos[(2n-1)u]\}, \quad (1.9)$$

and

$$P_{\Delta}^0(\theta) = \{B'_1 \sin 2u + B'_2 \sin 4u + \dots + B'_n \sin 2nu\} - \{B''_1 \cos 2u + B''_2 \cos 4u + \dots + B''_n \cos 2nu\}, \quad (1.10)$$

where the coefficients A'_i, A''_i, B'_i, B''_i are again as given in Equations 1.4, 1.5, 1.7, and 1.8.

Note that in contrast to Equations 1.3 and 1.6, the single-primed coefficients are now the weighting coefficients of the phase-antisymmetric array while the double primed coefficients pertain to the phase-symmetric array. The angle θ_0 , which determines the phase angle ϕ and hence the values of the modified weighting coefficients, indicates the tilted position of the notch of the difference pattern.

The two terms in braces in either Equation 1.9 or Equation 1.10 reveal that a tilted difference pattern can also be formed simply by combining the output of an appropriately weighted phase-antisymmetric array with that of an appropriately weighted phase-symmetric array. Again, the inherent phase quadrature between these two outputs must first be removed; in this case the two outputs must be subtracted rather than added in order to obtain a pattern tilted to the same side of the normal to the array as was the tilted sum pattern of Equation 1.3 or Equation 1.6. Further details of the doily system are contained in the Reference 5. ^[5] For the proper functioning of the imaging system it was necessary to construct a receiver, which has a ninety degrees phase-shifter, which works from 1-6MHz. This is the main focus of this thesis.

2.1.1 Array System Design

The transmit/receive array consists of about 160,000 elements formed from 1-3 piezoceramic composite transducer material and is 10 cm in diameter (see Figure 3). The array design parameters are given in Table I. The elements are electrically connected with an array interconnect board to form 1808 channels (reduction due to "doily" array technology). Each

channel (four per vertical stave) is connected to individual preamplifiers. The back of the array 1-3 composite material is bonded to an acoustically lossy backing material in order to eliminate reflection effects. The front of the array has a quarter-wave matching layer to optimize the bandwidth and a lens to weakly focus the acoustic energy. The array assembly is shown in Figure 4.

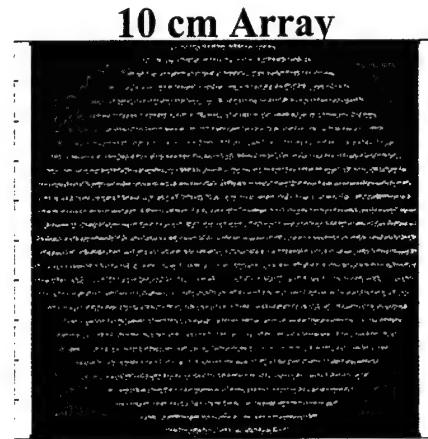


Figure 3. Array "Doily" Element Layout

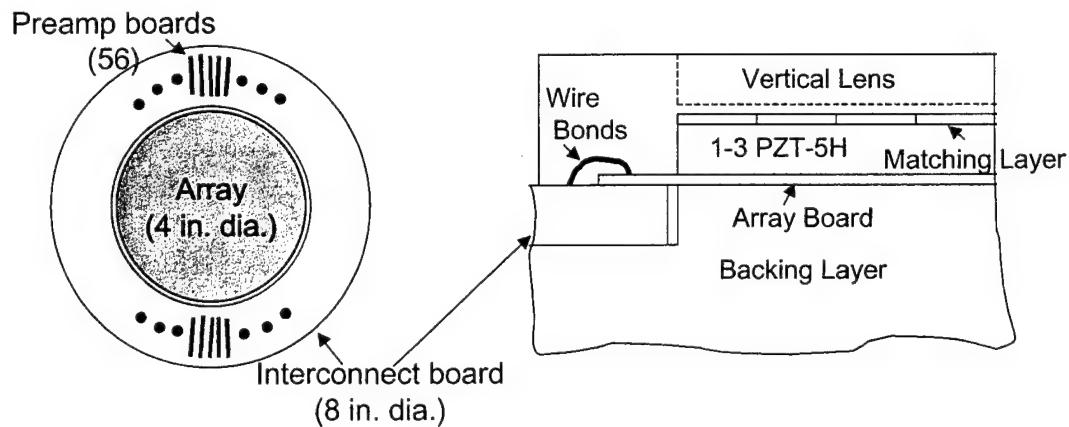


Figure 4. Array Conceptual Design

Table I: Array Design Parameters

Design Parameters	Values	Comments
Array size	9.93 cm. Diameter	Active diameter
Element vertical spacing	215.9 μ m	
Stave horizontal spacing	254 μ m	Smaller steering range
No. of elements	141,500 (approximate)	Estimated from area
No. of staves	392	
No. of channels	1568	4 per stave
Array thickness (active)	504 μ m	
Array thickness (total)	2.07 cm	Includes backing and matching layer

In order to steer in both planes, the array is divided up into vertical staves which are summed together with appropriate time delays to form steered beams in the horizontal direction. The elements in each horizontal stave are randomly assigned to the cos+, cos-, sin+, and sin- channels in order to reduce sidelobe levels at angles off the main axes. There are 55 sine and cosine lobes across the vertical extent of the array and each lobe is 0.18 cm wide. This means that there are about 8 rows per lobe, which is sufficient to approximate the sine/cosine functions.

2.1.2 Array 1-3 Composite Design

The active transducer material for the array consists of a 1-3 piezoelectric composite fabricated from 55% PZT-5H. Each element is made up of four sub-diced rods (30 micron kerf). The 1-3 composite design parameters are given in Table II.

Table II: Array 1-3 Composite Design Parameters

	1.1 Value
Piezoelectric material	PZT-5H
Volume fraction	55%
Matrix material (filler)	Polyurethane with phenolic microspheres
Element size	245 x 215.9 microns
Subdicing (rods per element)	2 x 2
Kerf	30 microns
Thickness	504 microns
Electrodes (gold pads)	224.0 x 185.9 microns
Matching layer	$\frac{1}{4}\lambda$ thick at 4.5 MHz
Diameter	10 cm

Due to the large size of the array, the final dimensions will be achieved by a mosaic of a number of smaller pieces of 1-3 composite. The ground side of the array will have a continuous electrode and the high electrical side will have rectangular electrode pads which will interface to an array interconnect board. The ground electrode continues around the side of the 1-3 composite to a thin border on the high side in order to connect the ground to the interconnect board. A matching layer is used on the transmitting side of the array in order to improve the bandwidth. The matching layer is designed to have an acoustic impedance of 4.5 Mrayls and be $\frac{1}{4}\lambda$ thick at 4.5 MHz.

2.1.3 Array Interconnect Board

The array elements are electrically connected via an interconnect board that consists of a thin Kapton substrate with gold traces and electrical contact posts deposited on one side. The gold posts protrude above the interconnect board to make electrical contact with the array elements when the array and the interconnect board are bonded together with non-conductive epoxy. The posts are connected with thin gold lines on one side of the Kapton. Each stave has four lines, one line for each “Doily” +cos, +sin, -cos, and -sin component. For each stave, all the “Doily” components are connected in parallel, so that there are only four channels per stave. The lines are insulated with a thin layer of Kapton. The lines are brought out to pads on two sides of the array where they are connected to an outer printed circuit board that is connected to the preamplifiers for each channel. A view of a corner of the array board layout is shown in Figure

36. The small circles are the contact posts. The figure shows the four pads that are used to check alignment. The four dots are designed to contact a square pad on the array which should electrically short them together if the array and interconnect board are aligned correctly.

2.1.4 Array Backing

The array and interconnect board assembly are bonded to a glossy tungsten-loaded epoxy backing material (2 cm thick). The backing is designed to match the acoustic impedance of the array so that almost all of the acoustic energy is transmitted through the array/backing interface and is then absorbed.

2.1.5 Acoustic Lens

A weak acoustic lens will be used to focus the acoustic energy in the ranges of interest. At some frequencies and ranges, the target will be in the far field and the remaining will be in the near field. The lens will be fabricated from a polymer material with the desired sound speed and density to obtain the required focusing. It will be fabricated directly onto the array matching layer.

2.2 Transmitter

The block-diagram for the transmitter is shown in Figure 5 below.

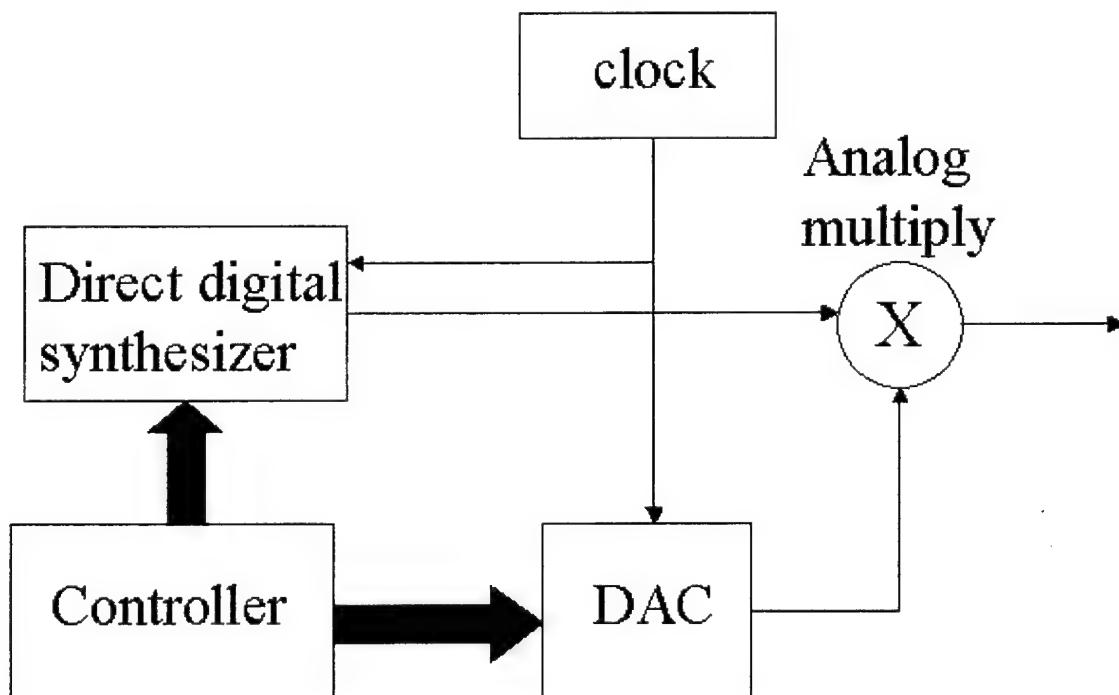


Figure 5. Block Diagram of the Transmitter

The purpose of the transmitter is to feed the doily array with appropriate input, so that it would generate a beam in the proper fashion required. The transmitter generates a sweep from 1-6 MHz and excites the transducer.

The transmitter consists of a Voltage Controlled Oscillator, a Time Gain Compensation Circuit, a T/R switch and a transducer interface (see Figure 6). The Voltage Controlled Oscillator generates a sweep from 1-6 MHz. The time gain compensation circuit is a variable gain amplifier that adjusts the amplitude of the signal in transmit mode for frequency dependent attenuation.

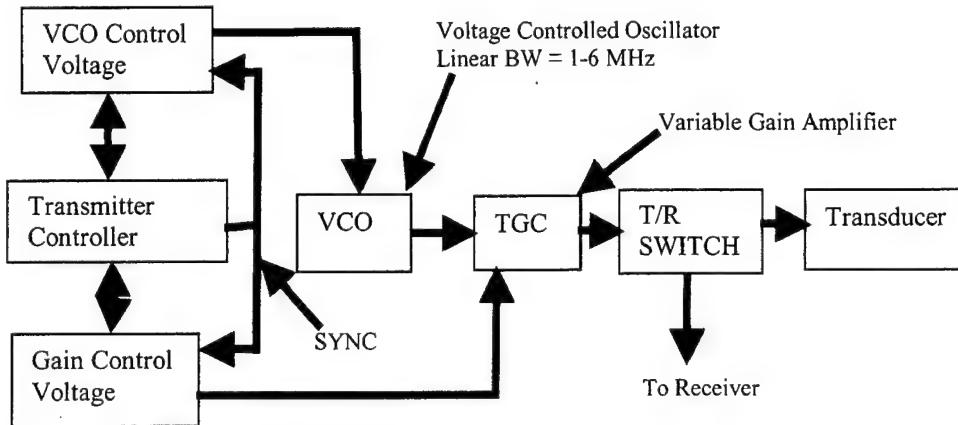


Figure 6. Functional Diagram of the Transmitter

This helps in generating the proper input to the transducer. The T/R switch does the switching operation between the receiver and the transmitter so that the receiver knows what is being feed into the transducer. The transducer is at the very front and it does the actual transmission and receiving. The detailed diagram of the transmitter with the actual chips is shown in Figure 7.

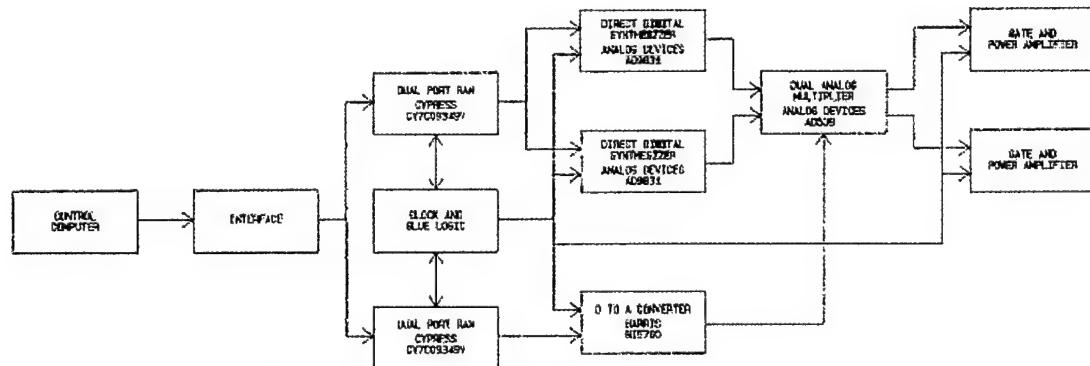


Figure 7. Detailed Diagram of Transmitter

2.3 Receiver

A block diagram of the receiver is shown in the Figure 8. Figure 8 has four different PCB boards for preamplifier and the phase shifter. Each board consists of eight channels of the receiver. Thus the figure shows 32 channels of the receiver. Each channel of the receiver consists of all the modules shown in Figure 1 at the input. The preamplifier is at the very front of the receiver. It interfaces directly with the transducer. Differential amplifier follows the preamplifier. As mentioned previously each channel of the receiver consists of two differential amplifiers. The

output of these two differential amplifiers goes into the input of each leg of the phase shifter. The output of the phase shifter than goes into a summing amplifier with differential output and a difference amplifier with differential output as shown in Figure 34. The output from the summer is interfaced to an Analog to Digital converter. After digitizing, the output interfaces to the imaging system, which forms the actual image displayed on the screen.

Eight channel receiver PCB was constructed and integrated in the system as shown in Figure 8. The next chapter discusses the analytic design and PSPICE modeling for one channel receiver.

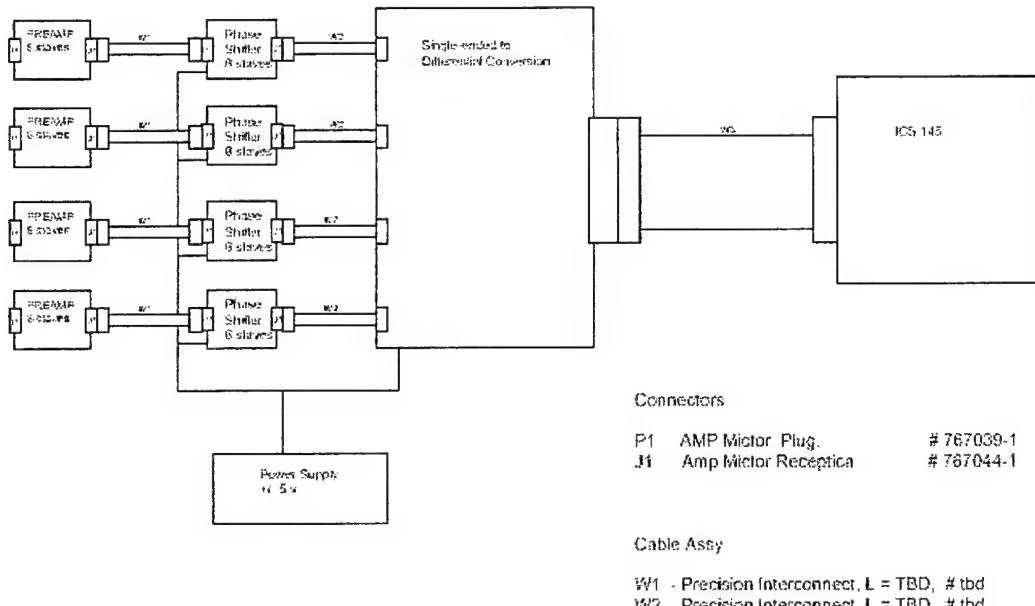


Figure 8. Receiver Block Diagram

3.0 FEASIBILITY STUDY FOR THE DOILY ARRAY IN MEDICAL ULTRASOUND APPLICATIONS

In order to further research in the two-dimensional Doily array, funding must be obtained. One approach is to leverage the Doily as a device for 3-dimensional imaging for medical applications. In this case the Doily must be shown to have sufficient imaging capabilities in the range less than 15 cm. A simulation created in junction with the Field program is used to investigate the performance of the Doily array. A full two-dimensional array with the same aperture and number of elements was simulated as a control to compare the performance of the Doily array.

The one centimeter Doily has been simulated to create images in the 30-50 cm. range but this range is excessive for medical ultrasound applications. In the imaging experiments each array was set up to image a set of point sources located 0.1 meters from the array face. Each array has the same aperture and number of "elements". The Doily elements are arranged in staves and each stave contains four types of elements: +sin, +cos, -sin, and -cos. Each element is of identical size and the kerf is the same in both arrays.

Creating synthetic images of point targets using the array simulation tested the performance of each array. Resolution capabilities of the arrays can be seen in the images. Plotting single cross-sections through the images performs a more detailed resolution analysis. The images in each array cover the same amount of 3D space, namely, 15 degrees in the horizontal and 22 degrees in the vertical. The horizontal range covers from -7.5 degrees to +7.5 degrees and the vertical angle goes from +5 to +25 degrees. The vertical angle is not symmetrical around 0 because of the operation of the Doily array. This constraint doesn't affect the performance of the full 2D array. This allows the results from the two array simulations to be more easily compared.

In both array types, the images were created by integrating over the range dimension to create 2-D data in the X,Y plane. The simplest evaluation of array performance is to image a single point target and look at the size of the point in the image. The size of the point return determines the resolving power of the array and for the Doily, this resolution is variable. Point targets for the full 2-D array are shown in Figure 9 and Figure 10 shows a point target imaged by the Doily array. Figures 11 and 12 shows a horizontal cross section through the point target in both array types. Figures 13 and 14 show a vertical cross section through the point target.

It is important to compare "apples to apples" when looking at the Doily array and the traditional 2-D array. The actual sampling rate of the Doily array is 12 MHz. but the Beamformer interpolates this rate 16x so the apparent sample rate is 192 MHz. In order for the 2-D array to be compared to the Doily, a sample rate of 192 MHz. must be used to make an accurate comparison. Also to utilize the full 2D array capacity, the first set of images were created using a transmit on all elements and the second set was created using a transmit on a single column of elements much like the Doily array.

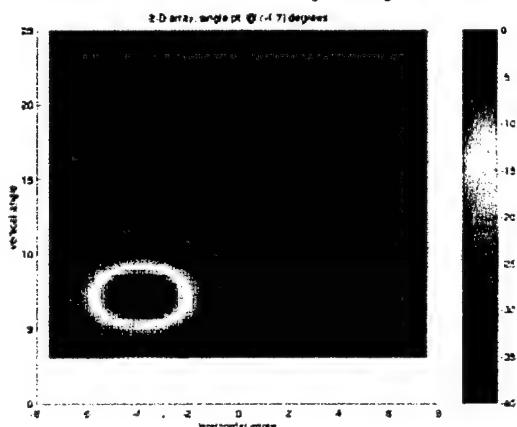


Figure 9. Full 2D Array

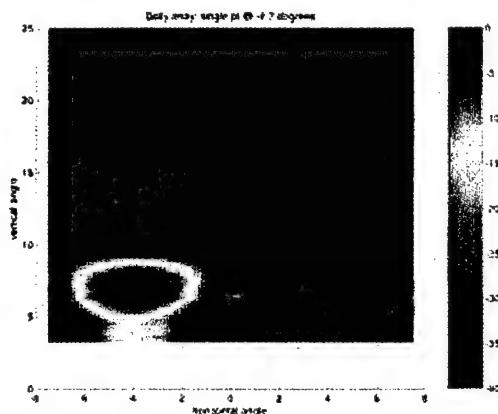


Figure 10. Square Aperture Doily Array

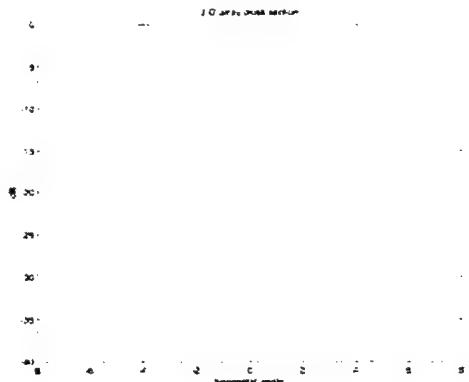


Figure 11. 2D Horizontal Cross Section

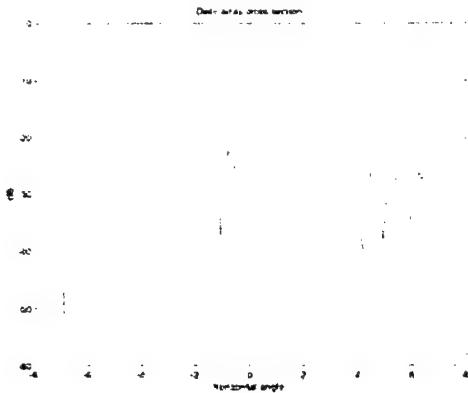


Figure 12. Doily Horizontal Cross Section

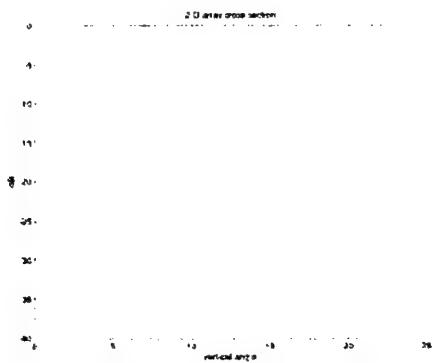


Figure 13. 2D Vertical Cross Section

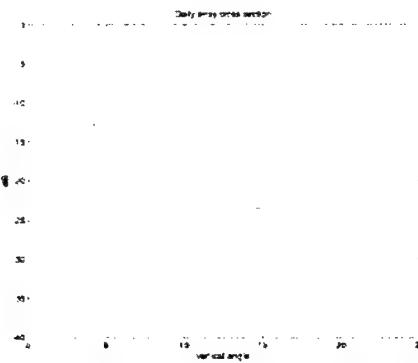


Figure 14. Doily Vertical Cross Section

The images are very similar for the two arrays if the points are located at 7° in the vertical. This angle corresponds to a frequency of 3.28 MHz, which explains why the point images are similar at this angle. If the angle is increased to 15° , the corresponding frequency is 1.65 MHz. and the image quality is significantly degraded. This is shown in Figures 15 and 16.

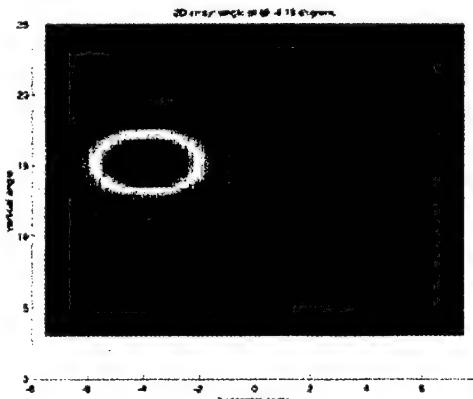


Figure 15. Full 2D Array

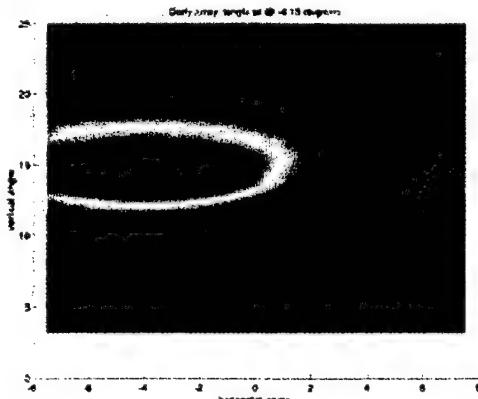


Figure 16. Doily Array

Multiple target simulations can shed more information on the nature of the image formation capabilities of the 1 cm. doily. Multiple targets are arranged so that the (X,Y) component of

their location has a constant interval. The Z component is adjusted to keep the distance from the array constant. In the following simulations, the image contains nine point targets are separated by 3° in both the horizontal and vertical directions (see Figures 17 and 18).

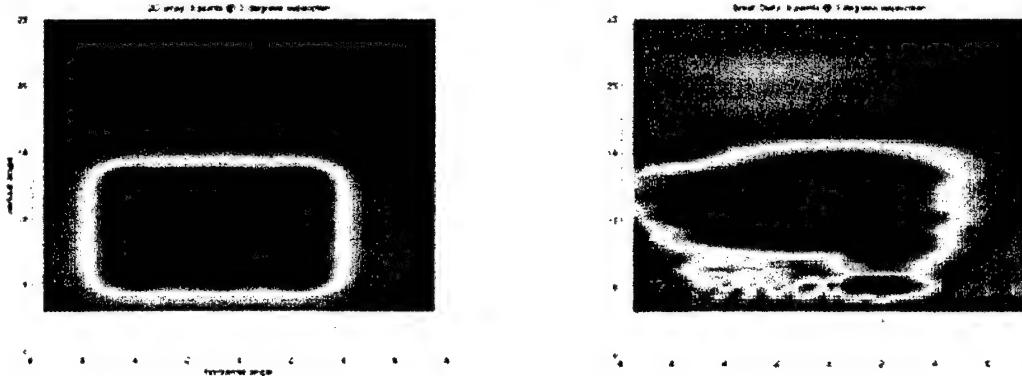


Figure 17. Multiple Target Image Generated with Full 2D Array

Figure 18. Multiple Target Image Generated with Doily Array

Further separating the point targets by 5° does not improve the quality of the doily image as shown in Figure 19.

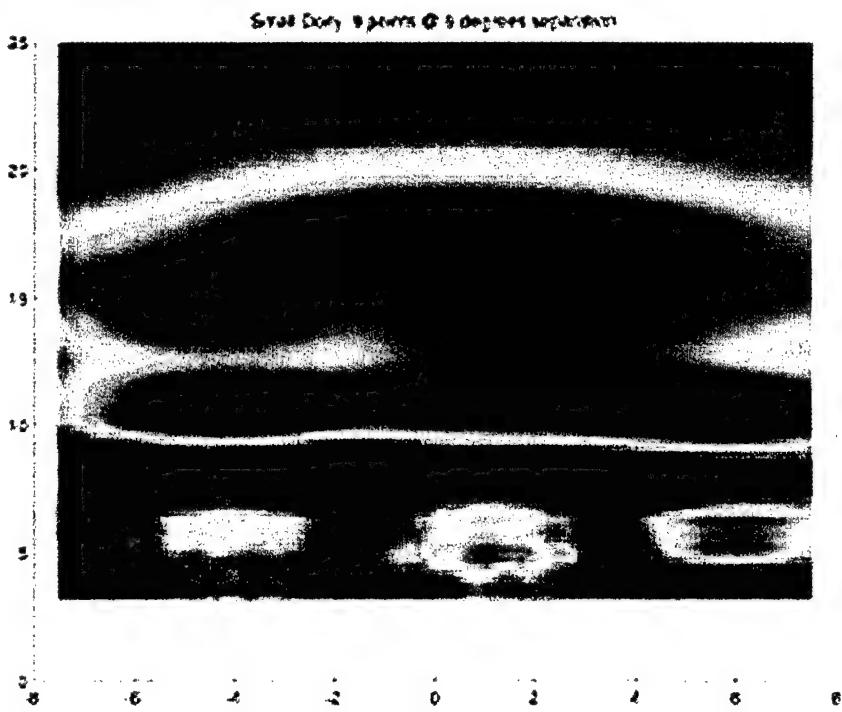


Figure 19. Multiple Target Images Generated with Doily Array

Alterations to the Doily array can be tested using the simulation software. Changing the array apodization can alter the array performance. Three types of array shading are tested and the results are compared. A one centimeter diameter array with a square aperture is compared to a similarly sized circular aperture array. These arrays are then compared to a Gaussian weighted circular aperture and a conventional two dimensional array. In this full 2D array, the transmit

aperture consisted of a single column of elements. This transmit compares closely to the Doily transmit aperture.

The effects of apodization on the image quality are tested using a single point target and a single transmit waveform based on the work of Tom Gabrielson. The point target is located at 0 horizontal and 7° vertical. Figure 20a shows the square aperture image. The side lobes are noticeable in both the horizontal and vertical directions. Figure 20b shows the circular aperture array imaging of the point target. Figure 20c is the resulting image from an array with a circular aperture and Gaussian shading. The shading is implemented by zeroing out single elements according to a spatial Gaussian distribution. Figure 20d is a point target imaged with a conventional 2D array operating at 3 MHz. This array is only transmitting on a single column of elements to make a more fair comparison with the Doily array. Finally, Figure 21 is a horizontal cross section through all of the above images. It shows the effects of apodization in more detail.

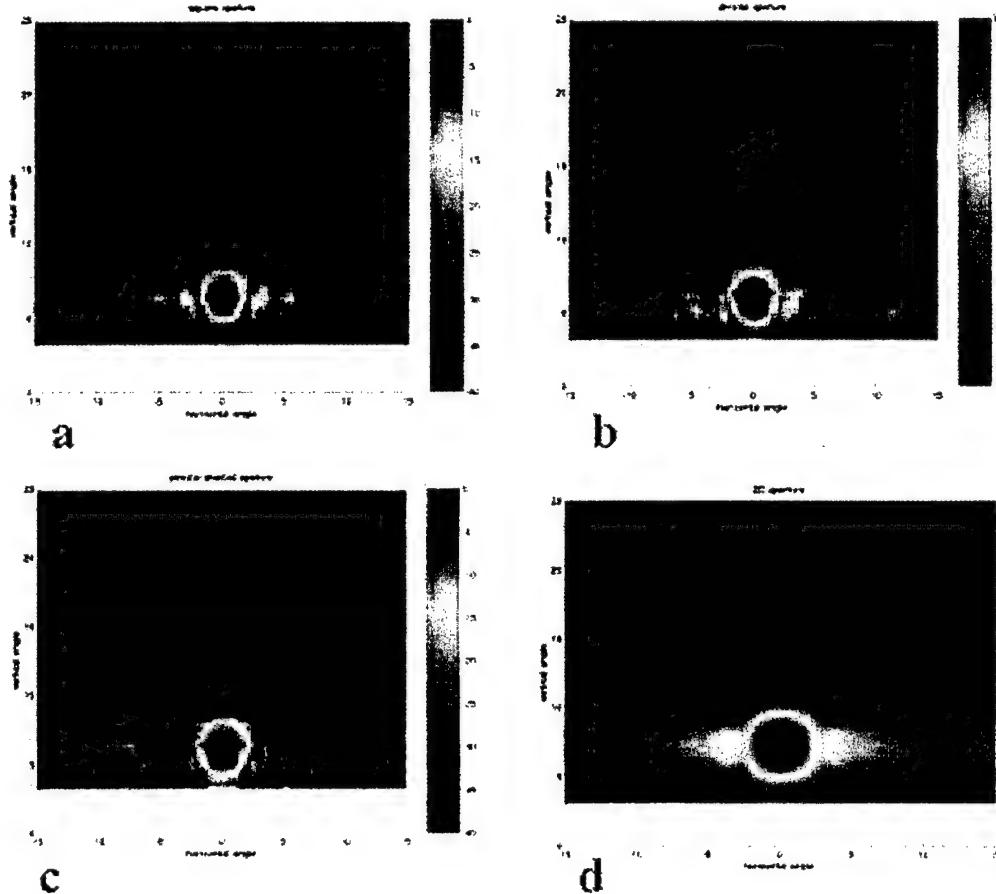


Figure 20. a. Square Aperture Doily Array, b. Circular Aperture Doily Array, c. Circular Aperture Doily Array with Gaussian Shading, d. Square 2D Array without Shading

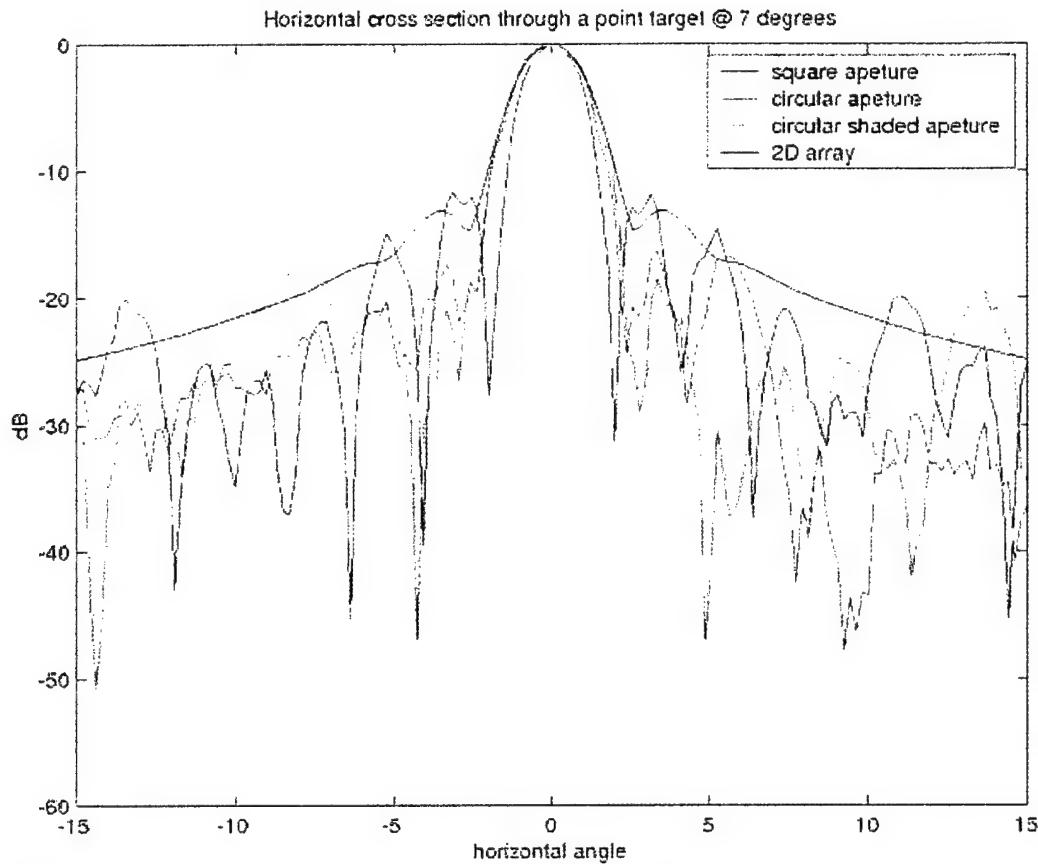


Figure 21. Horizontal Cross Section of a Point Target for all Four Array Apertures

The design of the transmit signal effects the image quality of the system. At this time, there are three simple transmit signals built into the simulation. The following Doily arrays have square apertures and no shading. The simplest signal is shown in Figure 22a and is a linear FM signal with uniform weighting across all frequencies. The second signal 22b is a linear FM with a linear weighting from 5 to 40 volts. Figure 22c shows the third transmit signal, which is weighted according to Tom Gabrielson's attenuation analysis. Each of the following images contain three point targets and the image quality is influenced by the transmit waveform. The output image is significantly dependent on the transmit waveform and should be an area of further research and experimentation.

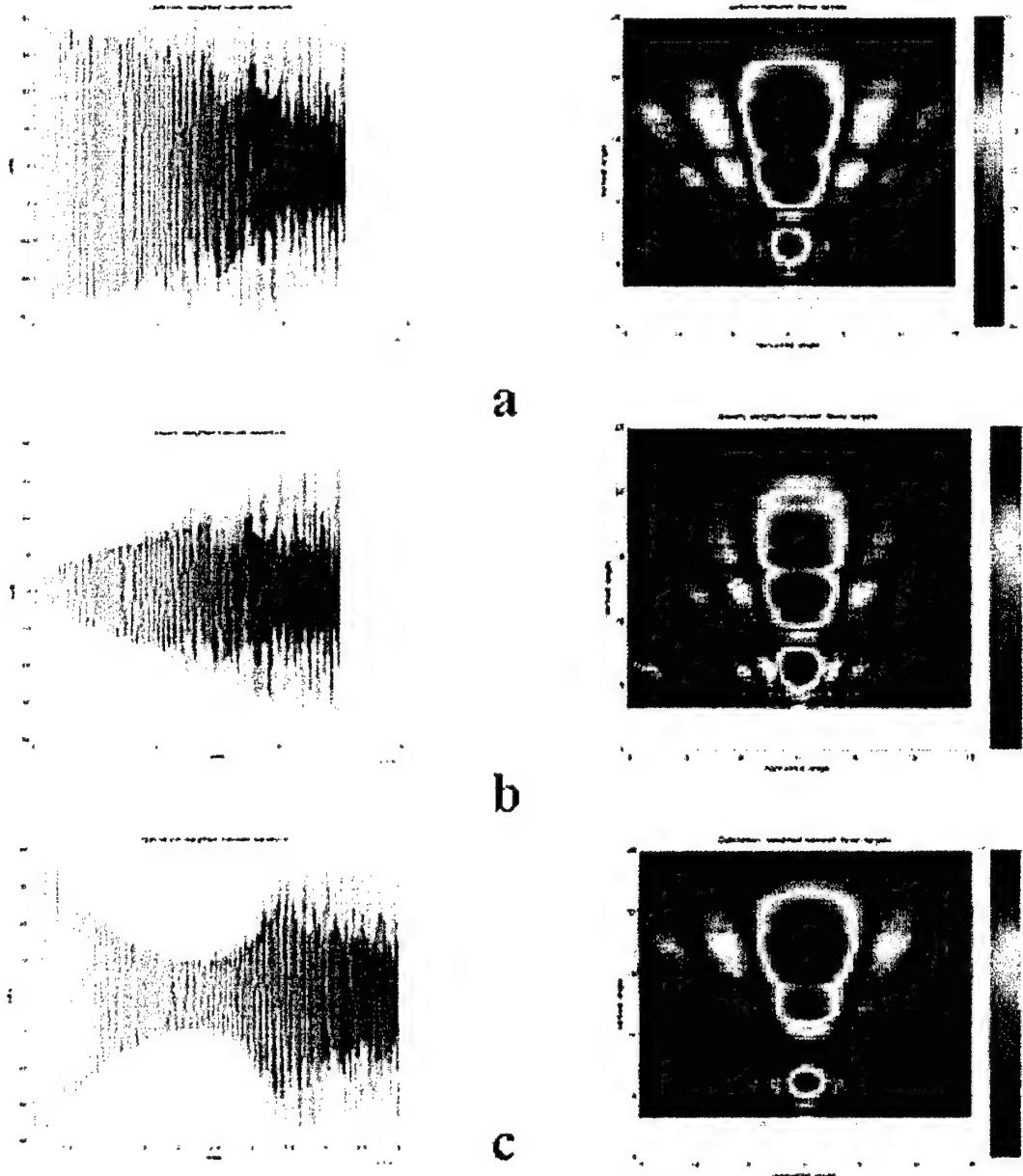


Figure 22. a. Uniform Array Transmit Signal and 3 Point Image, b. Linear Weighted Transmit Signal and 3 Point Image, c. Gabrielson Weighted Transmit Signal and 3 Point Image

4.0 FFT PROCESSING FOR IMAGE FORMATION

This section addresses the tremendous processing requirements of image formation in the hand-held sonar project. The two dimensional Doily array is capable of extracting 3D environmental information. The 3D imaging space has been defined in the proposal as having a range of 3-5 meters, the vertical, Doily, directions ranges 20° , and the horizontal range is 30° which is

controlled by a traditional time delay beamformer. The resolution specifications require a 1 centimeter resolution in the 3D image volume. Applying the Nyquist criteria, the 3D space must be sampled at twice the maximum resolution. Using 192 beams in the horizontal, 400 range bins and 214 frequency bins in the vertical, the 1 cm. resolution requirement is met but at a huge computational cost. Each frame will consist of $192 \times 400 \times 214 = 1.64E7$ data points (see Figure 23 and 24). Therefore to get 10 frames per second, $1.64E8$ data points must be computed per second.

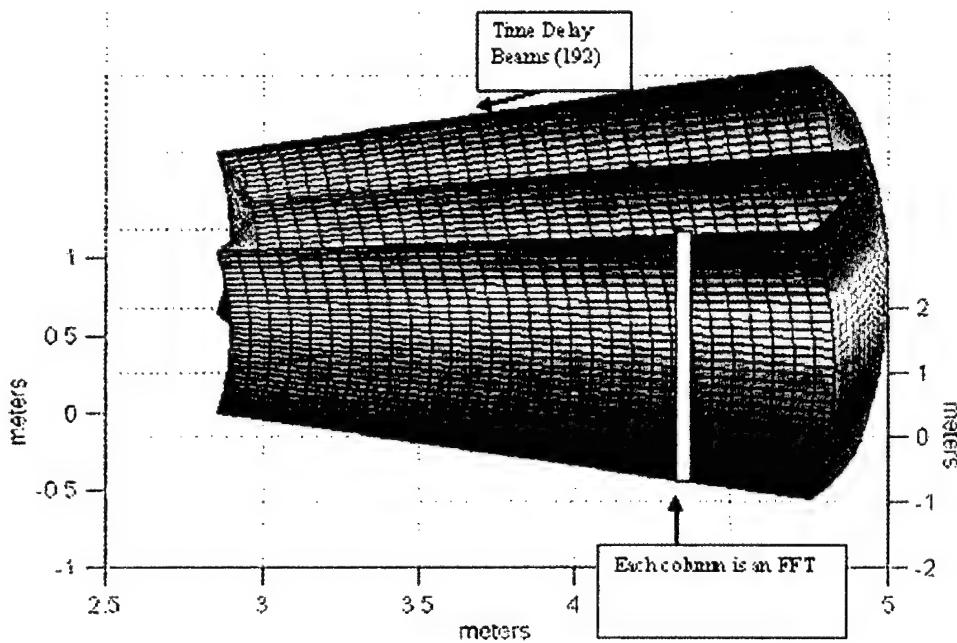


Figure 23. Description of Imaging Volume

different view of imaging volume

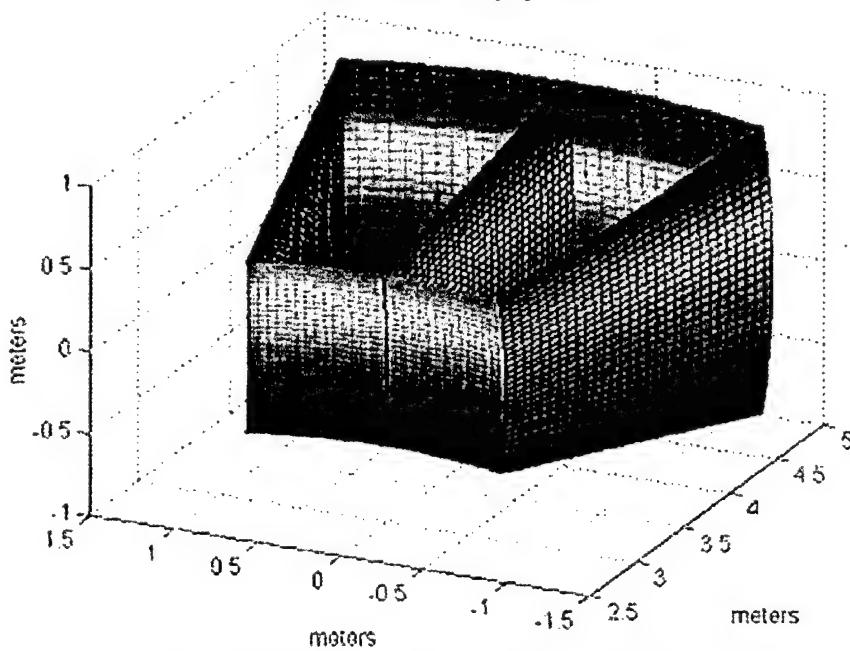


Figure 24. Different View of Imaging Volume

The data points in a 3D frame are computed by taking a large number of ffts. A single fft accounts for a single line in the 3D space. This “line” of data extends through the range/vertical plane to give 20° of coverage in the vertical dimension. Viewing the volume from the range/vertical plane, a single fft will appear as a single point, therefore, we will need to compute $192 \times 400 = 76800$ ffts to fill out the entire volume. Using the current state of the art hardware for PCI, a dedicated fft hardware board can perform a real 2048 point fft in 115.3 micro seconds. Therefore the ffts needed for a single frame at this resolution will take $115.3 \times 76800 = 8.86$ seconds for a frame rate of .113 frames per seconds for the fft processing.

The computational complexity can also be determined in terms of floating point operations per second (FLOPS). Using the *flops* command in MATLAB, the number of FLOPS required to implement a 2048 pt. Fft is 66971. The total flop count for fft operations in the image formation is $66971 \times 76800 \times \text{frame_rate}$ (using 10 fps as a low end estimate)=51.4 GigaFLOPS. A high quality general purpose DSP card based on PCI can perform at 840 MegaFLOPS.

4.1 Amplitude Shading

A one dimensional amplitude shading function is applied to the individual staves of the 2D Doily array. The aim of amplitude shading is to reduce the side lobe levels in the horizontal direction at the expense of increasing the main lobe width. The window used is a modified Hanning window with the form shown in Figure 25. Implementation of amplitude weighting is performed after the A/D conversion by multiplying the time element of each stave with the appropriate weighting constant.

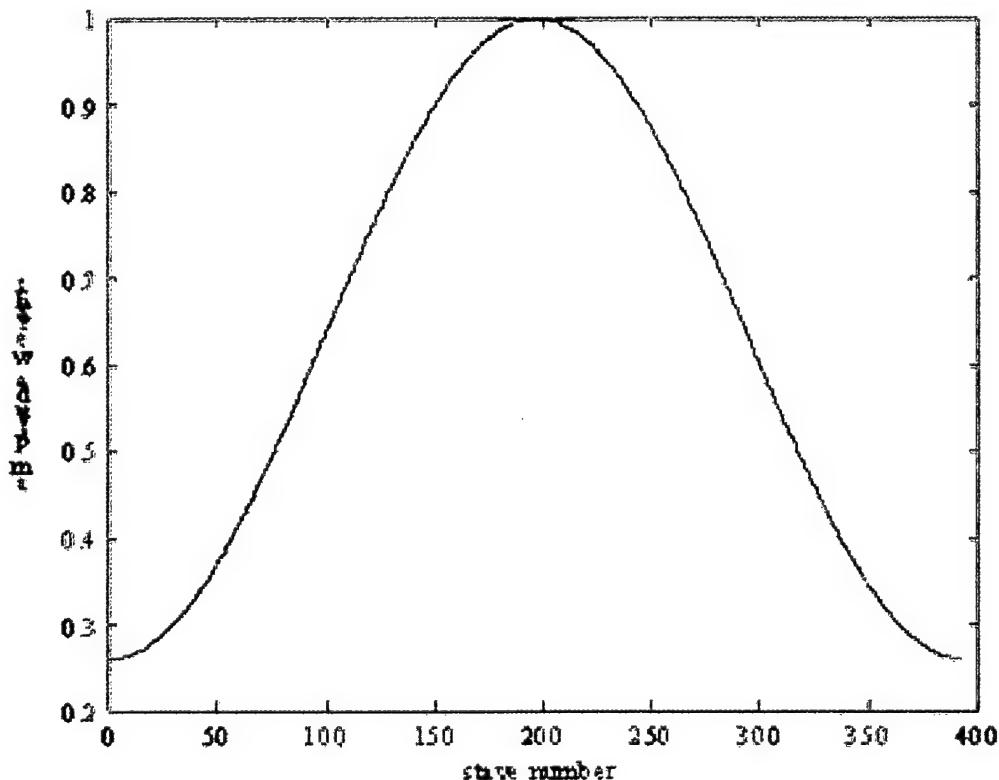


Figure 25. Hanning Window

The results of amplitude shading on a pair of point targets is shown in Figure 26. The red line shows the amplitude weighted array while the blue lines shows the unweighted array.

The differences between the shaded and unshaded array are clear. The shaded array returns lower side lobes with a slightly larger main lobe. The widening of the main lobe is minor compared to the side lobe suppression as far as image quality if concerned. The difference in image quality is shown by the two full images below. Each image is cut at -40 dB and the intensity is color coded.

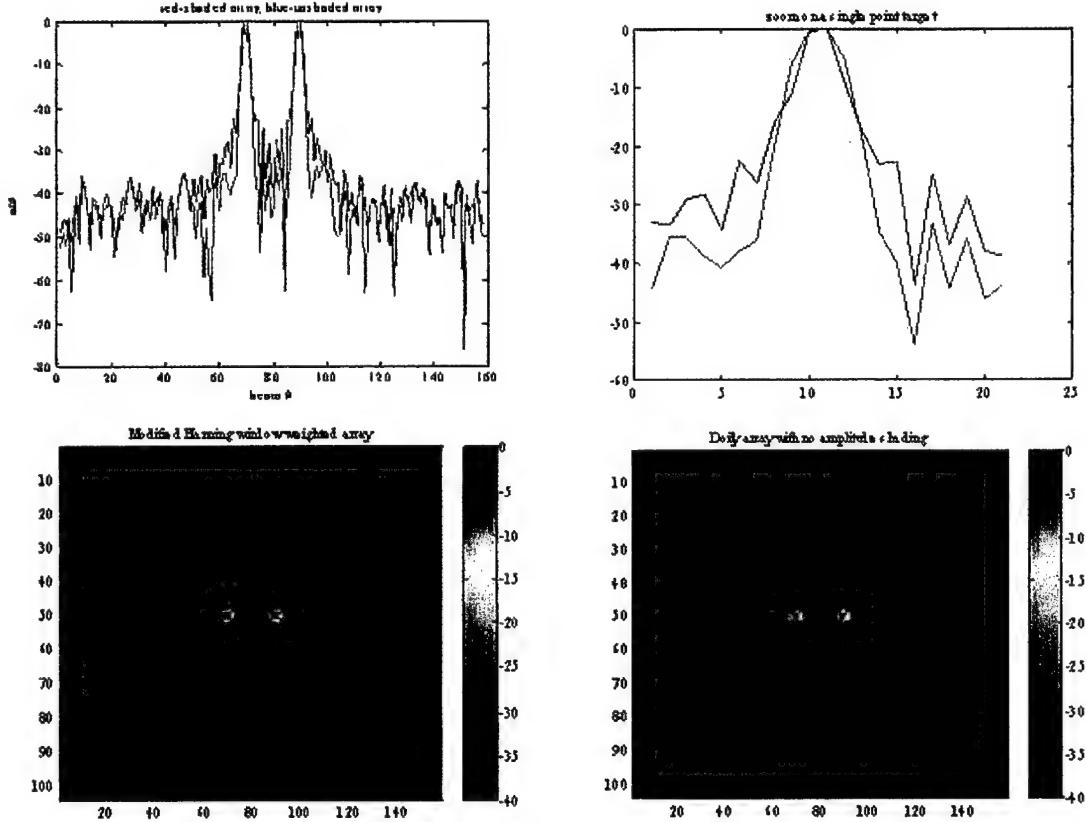


Figure 26. Illustration of the Effects of Amplitude Shading

4.2 Resolution Analysis

One of the main functions of the 2D Doily system simulation is to perform an analysis on the resolution limits of the array. This is not a simple task since the resolution of the Doily is variable and depends on the look direction in the vertical. In reality, it is the change in frequency that causes the change in resolution but the Doily look direction is directly related to frequency by:

$$\theta = \sin^{-1} \left[\frac{\theta_0}{\sin^{-1} \left(\frac{f}{f_0} \right)} \right] \quad (1.11)$$

Where f_0 is the design frequency of 5 MHz, and θ_0 is the design angle of 5 degrees. Resolution analysis is performed by imaging a set of point targets placed at variable space increments across the field of view. The resolution of the system is defined as the distance between two point targets at which the return signal shows a 3 dB dip between imaged targets.

The point target configuration used to test resolution consists of over 500 point targets non-uniformly spaced in the field of view. In the horizontal, three points are placed 0.5 cm. apart, followed by three points at 1 cm and then at 2 cm distances. These points are placed in the center of the viewing field for maximum sensitivity. Two other groups of points are places in the field of view. These points are separated by 2-6 cm and then final group is separated by 6-10 cm. In the vertical, groups of 5 points are separated by 1-5 cm. The closest points are placed near the bottom of the field of view where the beams are smaller and the resolution is better. The point target layout for resolution analysis is shown in Figure 27a.

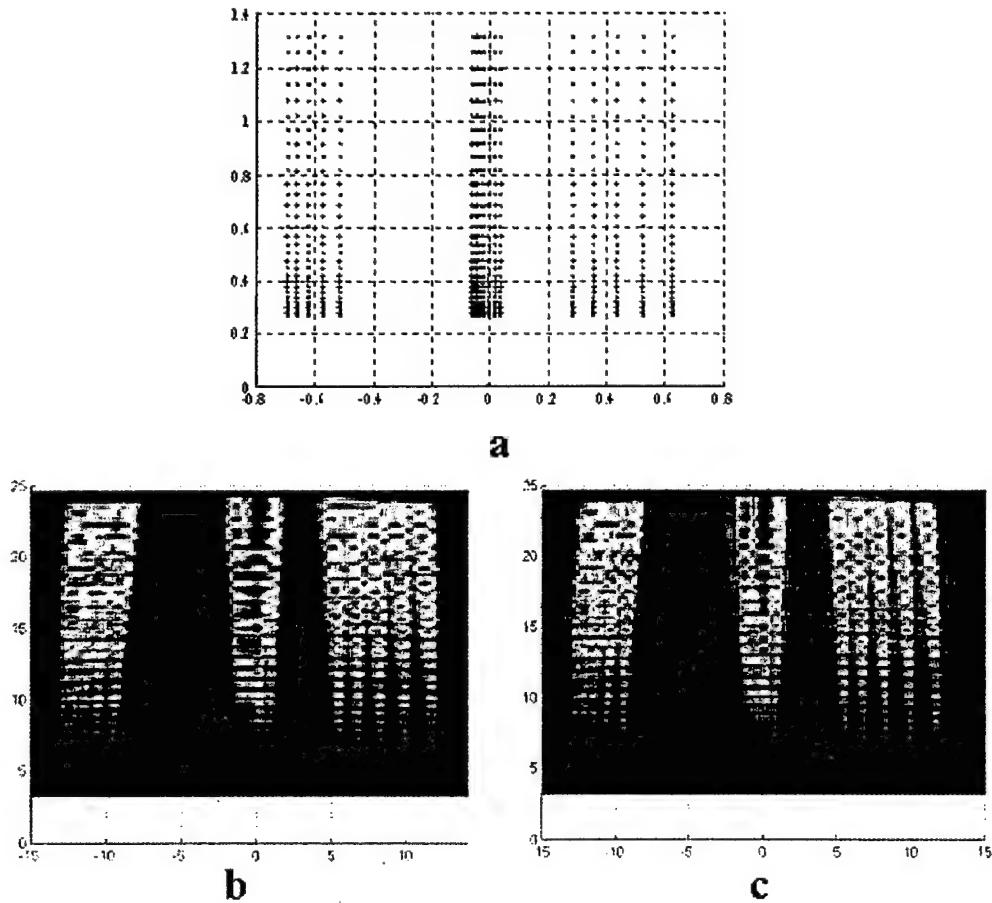


Figure 27 a. Point Target Layout, b. Hanning Shaded Array, c. Unshaded Array

The Hanning shaded array (Figure 27b) and the unweighted array (Figure 27c) resolution test patterns are shown below. The reduced side lobes in the shaded array are evident while the wider main lobe is less noticeable. A horizontal and vertical cross section is taken from the shaded and unshaded array to fully interpret the resolution capabilities of each array. The

horizontal cross section shows the resolving capabilities of the time delay beamformer. The point targets are divided into three physically separate sections. The first contains 5 targets separation distance varies from 3-6 cm for each pair in the group. The second section contains 9 targets. The first three are 0.5 cm apart followed by three spaced at 1 cm and then three spaced at 2 cm. The final grouping contains 5 targets separated by distances that vary from 7-10 cm in 1 cm increments. The shaded and unshaded arrays are shown in Figures 28 and 29.

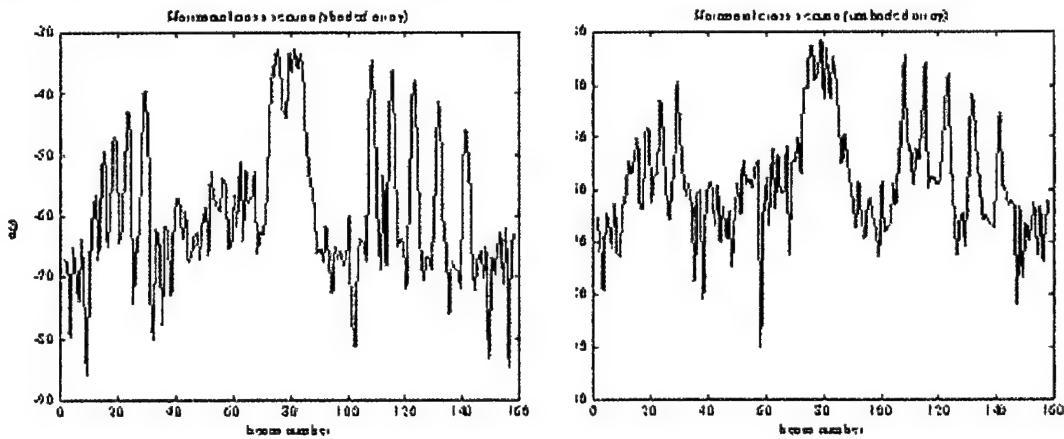


Figure 28. Horizontal Cross Section (shaded and unshaded responses)

The vertical cross section measures the resolution in the Doily direction. There are 31 vertical points in the resolution target. The first 6 points are situated with a 1 cm spacing and the following points increase there spacing by 1 cm in groups of five points. Therefore, the next five points are 2 cm apart and next set of five points have a spacing of 3 cm and the final group of points have a spacing of 6 cm.

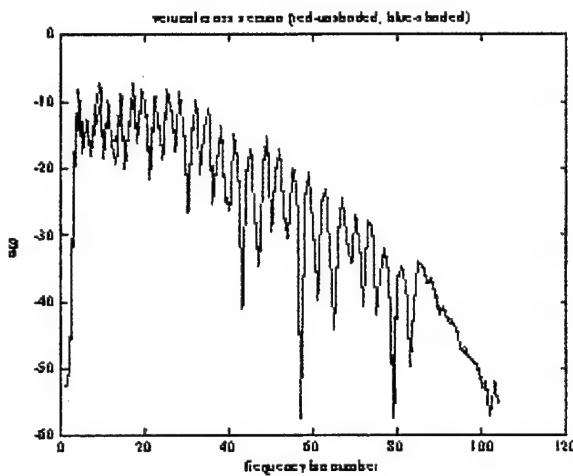


Figure 29. Vertical Cross Section (red:unshaded, blue:shaded)

The conclusion reached based on the resolution analysis is that the resolution in both the horizontal and vertical is between 1 and 2 cm. This measurement was determined at 3 meters and at a vertical angle of 5 degrees (highest frequency). In other words, the best resolution of the system is 1-2 cm. while the worst resolution has yet to be determined.

4.3 Imaging Capabilities

The next step in simulation is to demonstrate the imaging capabilities using distributed targets. At this time, a set of M-files has been written to create sphere targets and plate targets. These target models can be used in any combination to create more complex targets. There is a major concern with target realism since the Field program uses only point targets for target simulation. Therefore, a solid plate can only be achieved if point targets are placed infinitely close together. So far, a small number of plate targets in different combinations of position and reflectance have been tested in the simulation. The results of the simulation are shown in Figure 30.

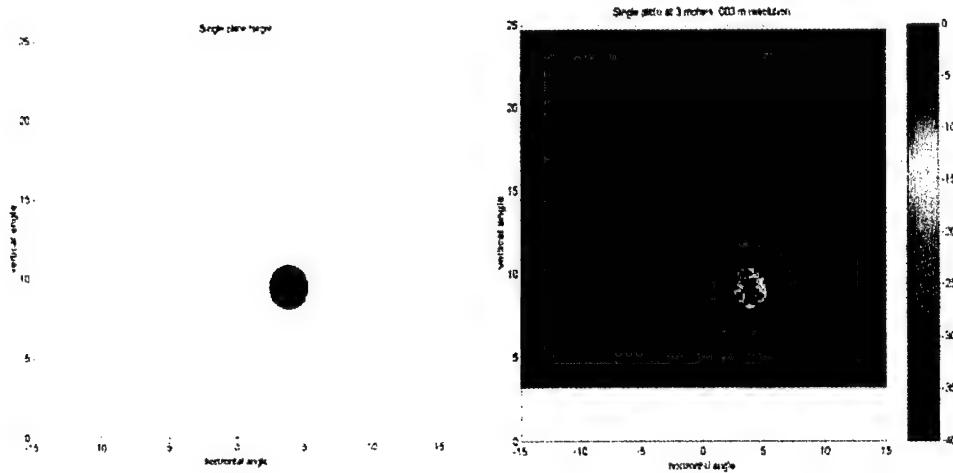
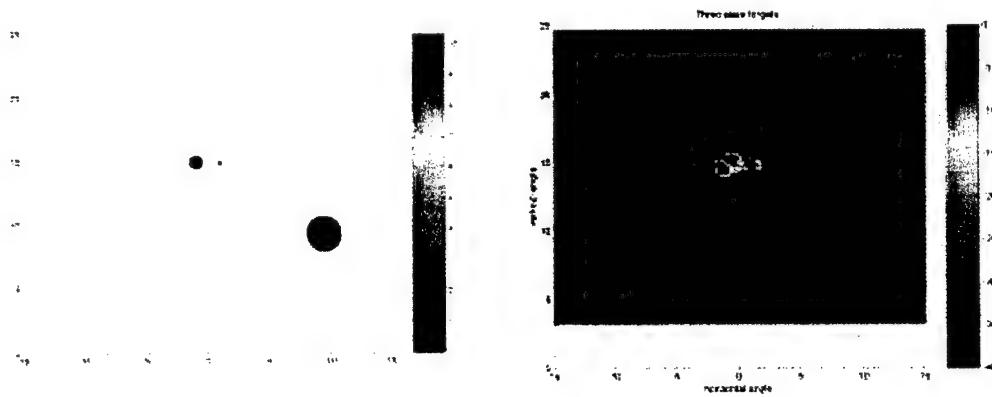


Figure 30. Single Plate at Range of 3 Meters with .003 Meter Resolution

The single plate target was created from roughly 3400 points reflectors with uniform amplitude. The target was placed at a distance of three meters and its diameter was 0.15 meters. The sample interval was 0.002 meters. Figure 31 shows three plate targets placed at different locations in the visual field. It consisted of three plate targets with diameters of 0.2, 0.06 and 0.02 meters. The arrangement of the targets does show the variable resolution of the system.



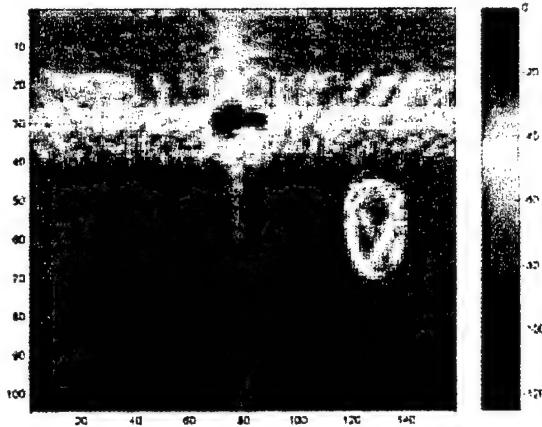


Figure 31. Three Plate Targets

The large target with a 0.1 target strength of the other smaller targets shows up at more than 40 dB down from the returns of the other two targets. For some reason the solid target appears hollow, where only the return from the outer rim is visible. Figure 32 shows a small plate on top of a large plate. The large plate is 0.2 meters while the small plate is 0.02 meters and has a return strength of 10X the large plate reflectance.

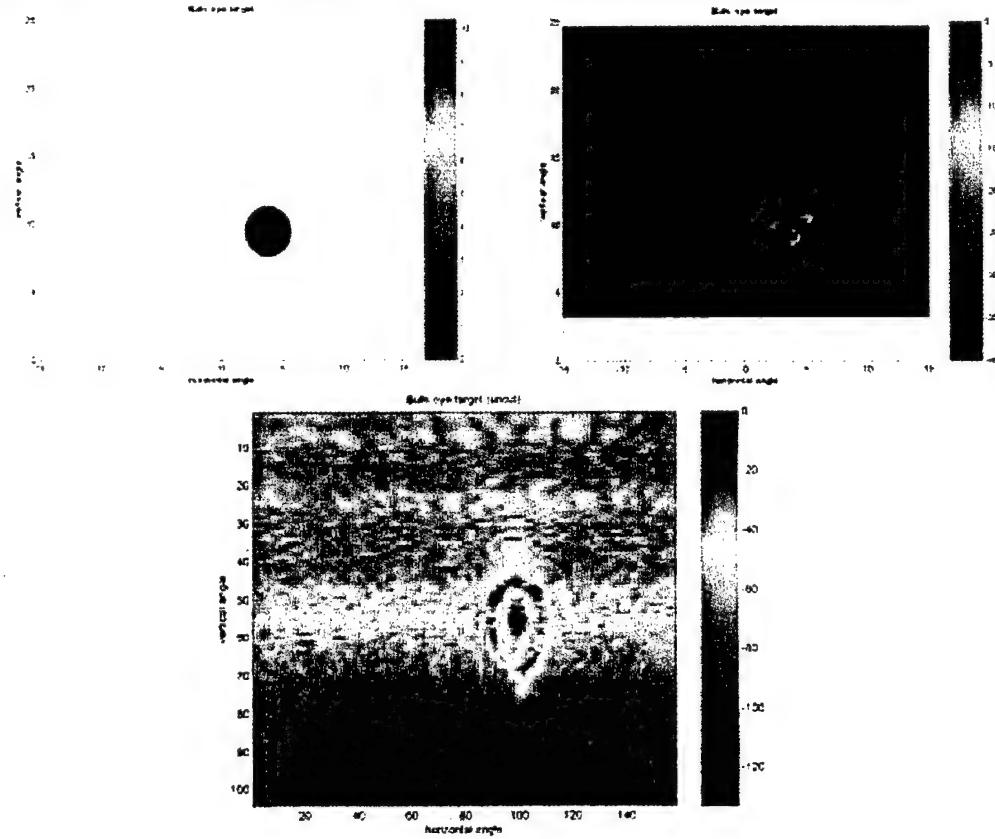


Figure 32. Bull's Eye Target

Decreasing the sample space between point targets can increase target realism at the expense of computation time. The next group of simulations combined multiple plate targets to create

pseudo-realistic targets shown in Figure 31. The target consists of a large plate target with a ring of smaller plate targets with a 20 dB increase in reflectance superimposed on the large plate. The smaller targets are 4cm. in diameter and the large plate size varies. In addition, the rear plate never "fills out" and we only get an outline of the plate. The target below consists of 82,000 point targets and took about seven days to run. The distance between point targets is 0.0025 meters.

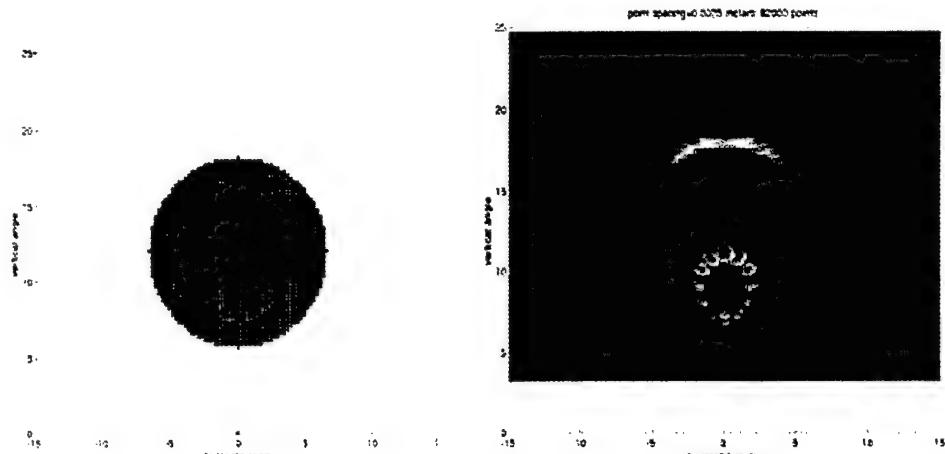


Figure 33. Combination Plate Target

There is a noticeable difference in return strength that seems to be correlated with vertical beam angle. The returns at lower frequency show a stronger target return than the higher frequency returns. This may be caused by the frequency dependent attenuation of the signal in water or may be a function of the angle of the plate target relative to the array. The cause can be tested by imaging two point targets at 5 and 25 degrees which corresponds to returns at 1 and 5 MHz.

4.4 Dynamic Range Analysis

This document describes the methodology for calculating the dynamic range, TVG and SNR requirements for the Diver Held sonar and presents the results of the analysis.

The method for determining the dynamic performance of the DHS receiver was to develop a system response model in MATLAB, assume a transmit forcing function and then optimize the forcing function to achieve the optimal response. The system response is given by the equation:

$$XF(f) + TRx - 2TL + TS + TRr$$

Where :

$XF(f)$ = Transmit Function

TRx = Transducer Transmit response

TL = One way transmission loss

TS = Target Strength

TRr = Transducer Receive Sensitivity

in dB

4.5 Transducer Characteristics

A Redwood spice model for the transducer was developed and a normalized frequency response for both Transmit Response (TRx) and Receive Sensitivity (TRr) was generated. These transfer function curves were read into MATLAB and 8th order polynomials were fit to the curves.

4.6 Transmission Losses

Transmission losses are affected by frequency, range and temperature. The transmission loss equation is given by:

$$TL = (R \times .001 \times \alpha \times f \div 1000)^2 + 20 \times \log 10(R)$$

Where : $\alpha = c4 \times T^3 + c3 \times T^2 + c2 \times T + c1 \times T$

$$c4 = -1.5e^{-8} \quad c3 = 9.11e^{-7}$$

$$c2 = -2.59e^{-5} \quad c1 = 4.937e^{-4}$$

4.7 Target Strengths

For this analysis the minimum target strength is given as -45 dB and the Maximum target strength is given as -5 dB.

4.8 Optimized Drive Voltage

A unity transmit function (0dB for all frequencies) was applied and the system response was calculated for a minimum target strength at minimum range. This transfer function was used as a basis for optimizing the drive voltage. The following algorithm was applied to the transfer function:

1. Take Inverse of transfer function
2. Normalize to 40 v rms (the maximum voltage of the transducer)
3. Calculate the system response to Minimum target Strength at Maximum range
4. Increase the drive voltage for all values that are below the Preamp noise floor + 20 dB
5. Clip the drive voltage at 40 v RMS
6. Calculate the system response to the new drive voltage to maximum target strength at minimum range
7. Add in the receiver fixed gain
8. Reduce the drive voltage on all values that exceed the maximum input voltage to the TVG amplifiers (0.281 vp-p).

The Simulation was performed for target strengths of -5 and -45 dB, for ranges of 1-3, 2-4 and 3-5 meters. All calculations were done at 10 deg C.

4.9 Dynamic Range Calculations

The dynamic range was calculated by taking the delta between the maximum received signal and the minimum received signal, using the optimized drive voltage and min and max target strengths. These values were calculated for each range bin, with a resolution of 1 cm. It is assumed that the TVG will correct for range dependent transmission losses and are not included in this calculation.

4.10 SNR Calculations

The Receiver SNR is the minimum signal to noise ratio of the receiver. The signal power is the received signal for the minimum frequency response of the minimum target strength at the maximum range. The noise power is computed by the referred input noise in a 10 kHz bandwidth. For this system, the input referred noise is $5nV/\sqrt{Hz}$, for a 10Khz bandwidth is – 126 dB.

4.11 Results

Figure 34 shows the Drive Voltage, System Response, Receiver SNR, and dynamic range for ranges of 1-3m, 2-4m and 3-5m. It should be noted that the SNR curve is for a single channel and does not include the 26 dB coherent gain of the beamformer. Table III shows the SNR & Dynamic range for the systems at the indicated ranges assuming a 20 dB receiver gain.

Table III: SNR and Dynamic Range vs. Range

Range	SNR (dB)	Dynamic Range (dB)
1-3 m	-5 to 25	40 to 70
2-4	2 to 20	47 to 57
3-5	-12 to 20	57 to 72

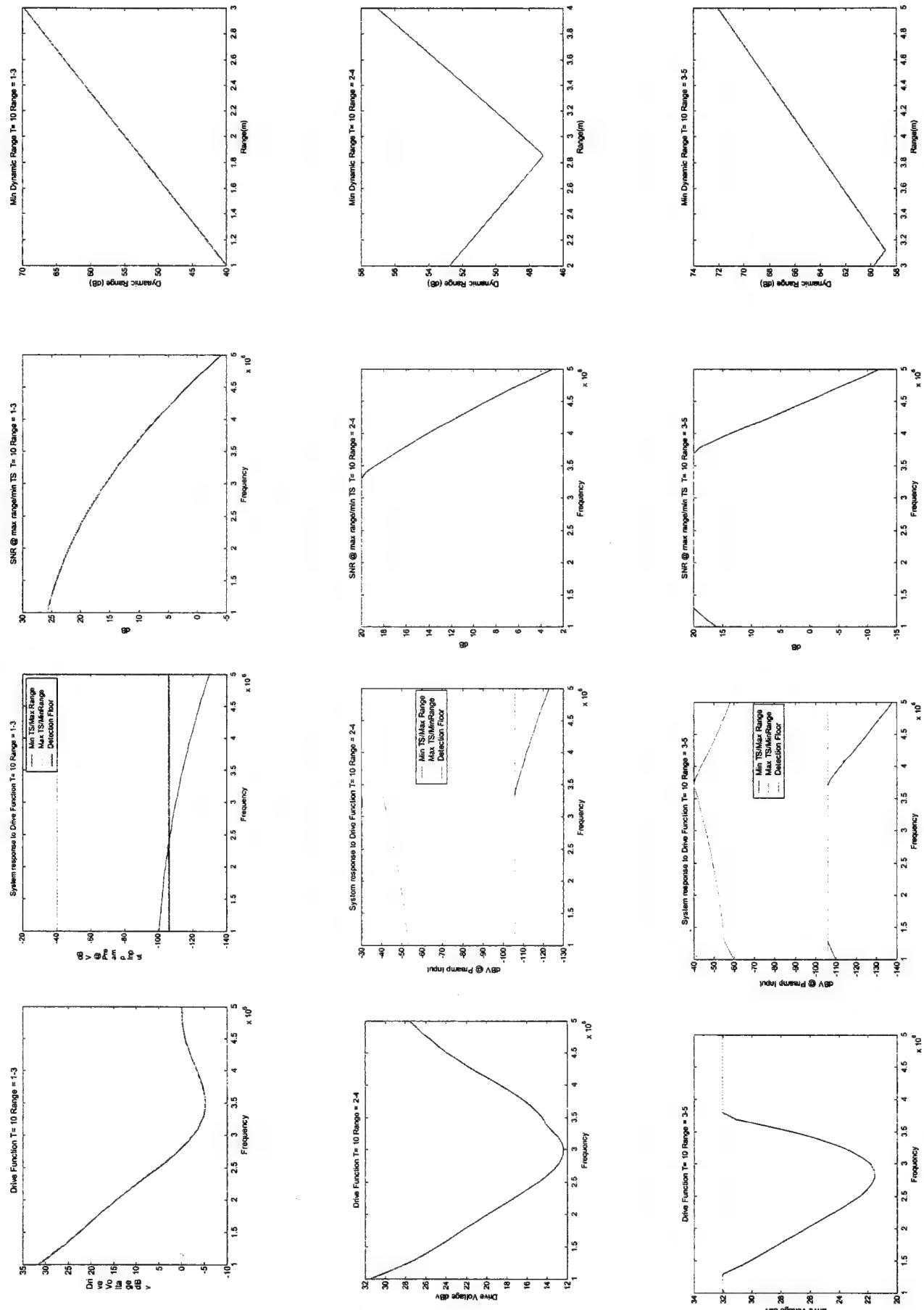


Figure 34. Drive Voltage, System Response, SNR, and Dynamic Range vs. Range

5.0. CIRCUIT DESIGN

In this section, the following topics are discussed:

- Analytic Design
- PSPICE modeling
- Expected results

5.1 Analytic Design

The analytic design was done for the following specifications.

- ✓ A pre-amplifier with a gain 10 that works from 1KHz-6MHz.
- ✓ A differential amplifier that works from 1 MHz-6MHz.
- ✓ A $\Pi/2$ phase shifting network that works from 1MHz-6MHz.
- ✓ A summing amplifier, with a differential output, for the output of the phase shifter.
- ✓ A difference amplifier, with a differential output, for the output of the phase shifter.
- ✓ Integration of the entire system on a four-layer PCB board.
- ✓ Design of an eight-channel receiver PCB board with AMP connectors.

Figure 35 illustrates the schematic of the circuit.

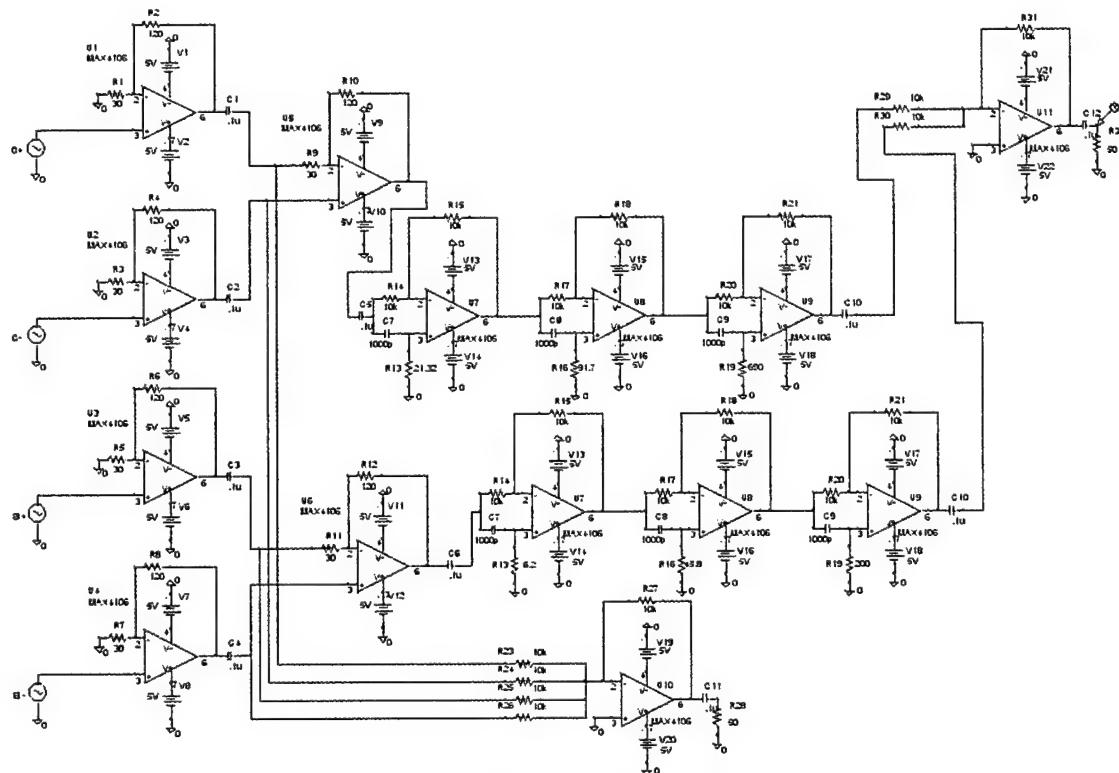


Figure 35. Analog Front End

The circuit consists of preamplifiers, differential amplifiers, phase-shifter and a summing amplifier. The circuit represents one complete channel. As can be seen from the Figure 331, one channel consists of four preamplifiers, two differential amplifiers, one phase-

shifter and one summing amplifier. The circuit as shown above was assembled on a brass-board and tested. In a design revision, the output stage was configured as a differential output stage. The output stage has both a differential amplifier and a summing amplifier. The outputs of the differential amplifier and the summing amplifier are differential.

Also, the preamplifier where assembled on a separate PCB. The modified circuit is shown in Figure 36.

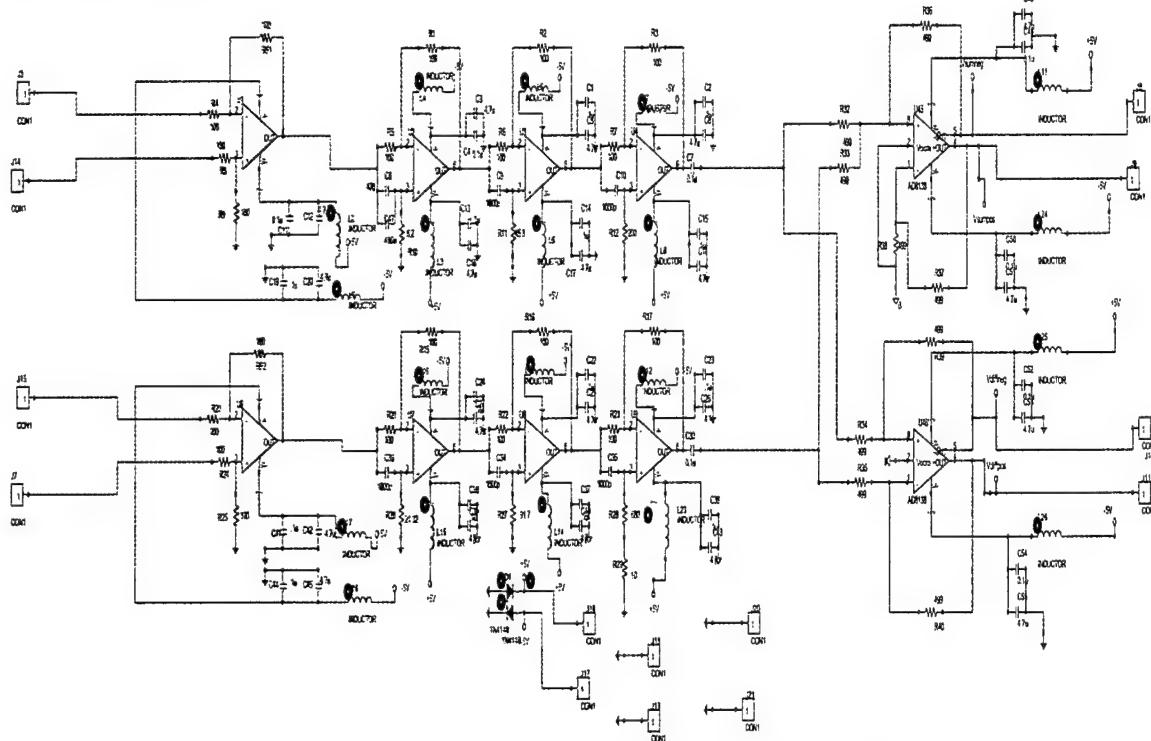


Figure 36. Receiver with Differential Output

All the operational amplifiers used, except for the differential output stage, for the above circuits are current feedback op-amps (AD8005). The operational amplifiers used for the differential output stage was AD8138. The AD8005 is a current feedback amplifier. The AD8005 is an ultra low power, high-speed amplifier with a wide signal bandwidth of 170 MHz and slew rate of 280 V/μs.^[9] This performance is achieved while consuming only 400 μA of quiescent supply current. These features increase the operating time of high-speed battery-powered systems without reducing dynamic performance. The current feedback design results in gain flatness of 0.1 dB to 30 MHz while offering differential gain and phase errors of 0.11% and 0.4°. Harmonic distortion is low over a wide bandwidth with THDs of -63 dBc at 1 MHz and -50 dBc at 10 MHz. The AD8005 is characterized for +5 V and ±5 V supplies and will operate over the industrial temperature range of -40°C to +85°C. To summarize AD 8005 has the following features.

AD 8005 Features^[9]

1. Ultra low Power

400 mA Power Supply Current (4 mW on ± 5 V_S)

Specified for Single Supply Operation

2. High Speed
 - 270 MHz, -3 dB Bandwidth ($G = +1$)
 - 170 MHz, -3 dB Bandwidth ($G = +2$)
 - 280 V/ms Slew Rate ($G = +2$)
 - 28 ns Settling Time to 0.1%, 2 V Step ($G = +2$)
3. Low Distortion/Noise
 - 63 dBc @ 1 MHz, $V_O = 2$ V p-p
 - 50 dBc @ 10 MHz, $V_O = 2$ V p-p
 - 4.0 nV/ \sqrt{Hz} Input Voltage Noise @ 10 MHz
4. Good Video Specifications ($R_L = 1$ kV, $G = +2$)
 - Gain Flatness 0.1 dB to 30 MHz
 - 0.11% Differential Gain Error
 - 0.4° Differential Phase Error
5. Applications
 - Signal Conditioning
 - A/D Buffer
 - Power-Sensitive, High-Speed Systems
 - Battery Powered Equipment
 - Loop/Remote Power Systems
 - Communication or Video Test Systems
 - Portable Medical Instruments

Current feedback amplifiers are considerably different than the conventional voltage feedback amplifiers. Current feedback amplifiers (CFB) offer advantages over voltage feedback amplifiers (VFB), but there are some important differences in the circuit topologies, which have to be taken into consideration. The VFB op-amp is certainly most popular in low frequency applications, but the CFB op-amp has some advantages at high frequencies. A comparison between the two is shown in Figures 37 and 38.

5.1.1 Comparison of VFB and CFB

Analytical Comparison of the Voltage Feedback and Current Feedback Amplifiers

The conventional voltage feedback op-amp has three stages: an input stage configured as a differential amplifier, a gain stage, and an output stage.^[6]

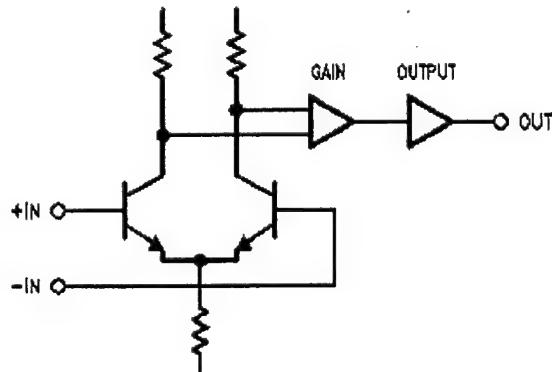


Figure 37. Voltage Feedback Amplifier

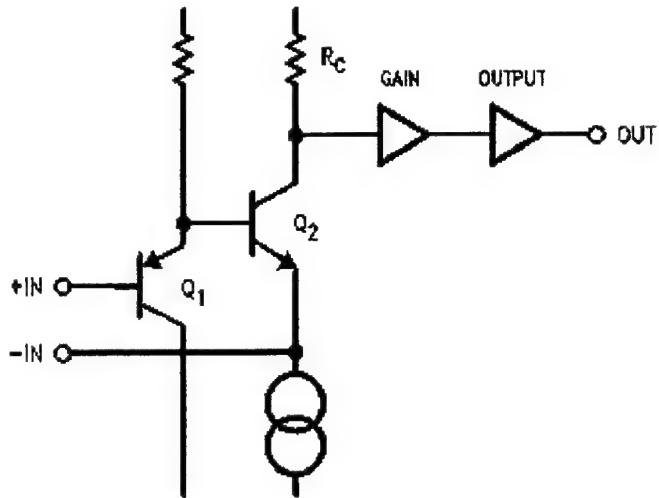


Figure 38. Current Feedback Amplifier

The differential amplifier provides two symmetrical inputs. The open loop gain is independent of the set gain and we have the situation of the gain-bandwidth product being constant. Hence when the op-amp is set for higher gain the roll-off starts at a lower frequency. The current feedback amplifier has the input stage configured as an Emitter follower (or a source follower for a FET input). This makes for an inherently faster response because the input stage works at a unity voltage gain and hence has a less Miller capacitance. This can be explained as follows.

The Miller capacitance (c) of a transistor is given by^[10]

$$c = c_e + c_c (1 + g_m R_L) \quad (2.1)$$

Where c_e and c_c are the emitter capacitance and the collector capacitance respectively. R_L is the load resistance and transconductance (g_m) is dependent on the set gain of the amplifier. If set gain is less than g_m is less, which in turn leads to less Miller capacitance. Since the gain of the very first stage (input stage) of a current feedback amplifier is one, the Miller capacitance for a current feedback amplifier is much less than that for voltage feedback amplifier (the gain of the first stage of the voltage feedback amplifier is high because it is configured as a differential amplifier). Since the Miller capacitance is less the rise and fall times are much less and these makes for an inherently faster response. The current feedback amplifiers are optimized for speed and have a comparatively low open loop gain. The bandwidth of the current feedback amplifier is almost independent of the set gain.

Also, the inverting input feeds into the emitter of the second stage. This being a low impedance node (because of low emitter resistance), the input impedance of the inverting input is very low. The non-inverting input feeds into the base of the first stage. This being a high impedance node (because of the high base resistance), input impedance of the non-inverting input is high. This is a fundamental difference between a CFB and a VFB op amp, and also a feature, which gives the CFB op amp some unique advantages.

The feedback function in a current feedback amplifier is accomplished by injecting current into the emitter. This current then flows through the collector resistor and produces a voltage proportional to the injected current. This feedback does not affect the

very first stage. This stage operates as an open loop buffer with a voltage gain close to one.^[7] The inverting input of the current feedback amplifier is inherently sensitive to capacitance. The reason for this is that at higher frequencies the gain of the stage is increased and at this gain the amplifier becomes unstable.

The gain in the current feedback amplifier is set by R_F and R_G but with the provision that the resistor values are right for the amplifier. This is necessary because the gain of the feedback stage is set by the impedance on the inverting input. When set gain is low, on some current mode amplifiers the Gain Vs Frequency curve tends to peak at high frequencies. This can be explained as follows. For lower gains the gain setting resistor R_G is larger and at some frequency the stray capacitance of the inverting input node, in parallel with R_G becomes dominant and increases the gain of the amplifier. When R_G is low, as it is for high gain settings, this crossover frequency becomes so high that it falls outside the amplifier's frequency range and therefore is of no consequence.^[8]

Unlike conventional voltage feedback op amps, the choice of feedback resistor has a direct impact on the closed-loop bandwidth and stability of a current feedback op amp circuit. Reducing the resistance below the recommended value makes the amplifier more unstable. Increasing the size of the feedback resistor reduces the closed-loop bandwidth. In power-critical applications where some bandwidth can be sacrificed, increasing the size of the feedback resistor will yield significant power savings. A good example of this is the gain of +10 case in AD 8005, as shown in Figure 38.^[9] Operation from a bipolar supply (± 5 V), the quiescent current is 475 mA (excluding the feedback network). The recommended feedback and gain resistors are 499 ohm and 56.2 ohm respectively. In order to drive an rms output of 2 V, the output must deliver a current of 3.6 mA to the feedback network. Increasing the size of the resistor network by a factor of 10 as shown in Figure 39 will reduce this current to 360 μ A. The closed loop bandwidth will however decrease to 20 MHz.

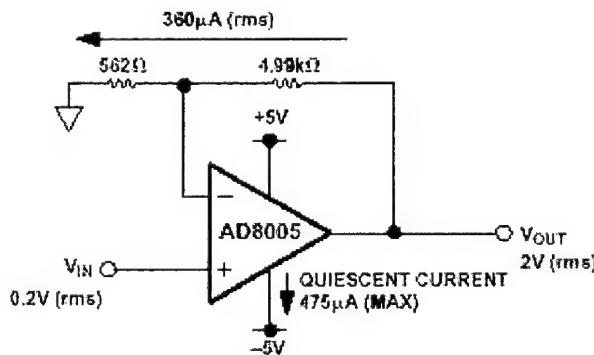


Figure 39. Saving Power by Increasing Feedback Resistor Network

5.1.2 Pre-Amplifier

The schematic for the pre-amplifier is shown in Figure 40.

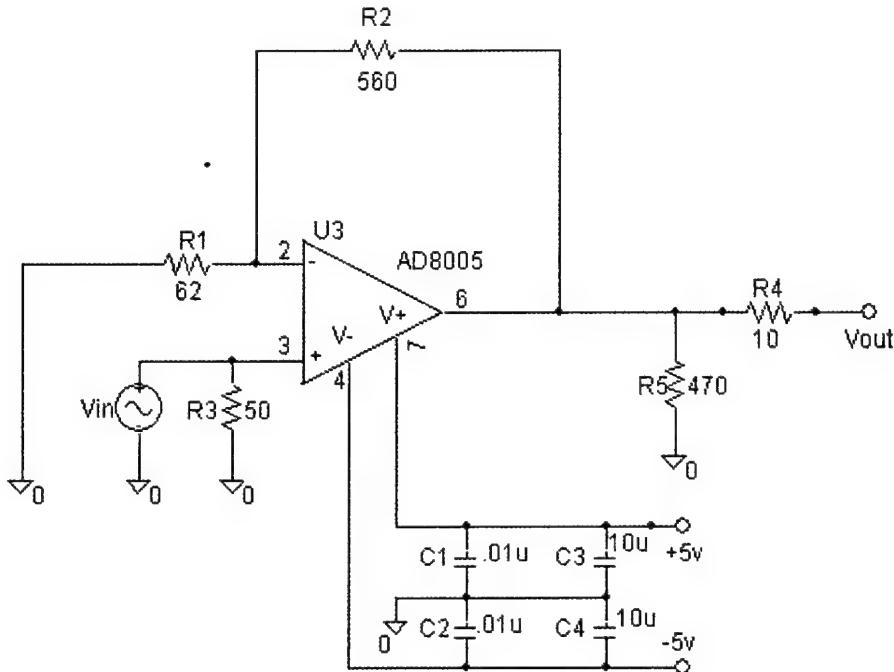


Figure 40. Pre-amplifier

The pre-amplifier used above gives a gain of 10. It is also flat in the required bandwidth. The pre-amplifier shown above has a flat frequency and a phase response from 1KHz to 6MHz as is required. The pre-amplifier was tested in PSPICE for gain and phase requirements. After that, the pre-amplifier was assembled on an Elantec board using the AD8005 op-amp and tested. The integration of pre-amplifier on the same PCB board as the phase-shifter and the summer was not done. Instead a separate PCB board containing only the pre-amplifiers has to be made. A PCB board with the differential amplifier, the phase-shifter and the summer was made and tested successfully.

5.1.3 Phase-shifter

Wide-band 90° phase-shift networks have a single input and two output ports.^[11] Both outputs maintain a constant phase difference of 90° within a prescribed error over a wide range of frequencies. The overall transfer function is all-pass. These networks are widely used in the design of single-sideband systems and in other applications requiring 90° phase splitting.

Bedrosian^[12] solved the approximation problem for this family of networks on a computer. The general structure is shown in Figure 41, and consists of N and P networks. Each network provides real-axis pole-zero pairs and is all-pass. The transfer function is of the form

$$T(s) = \{(s - \alpha_1)(s - \alpha_2) \dots (s - \alpha_{n/2})\} / \{(s + \alpha_1)(s + \alpha_2) \dots (s + \alpha_{n/2})\} \quad (2.2)$$

where $n/2$ is the order of the numerator and denominator polynomials. The total complexity of both networks is n . Real-axis all-pass transfer functions can be realized using a cascade of passive or active first-order sections. Both versions are shown in Figures 42 and 43.

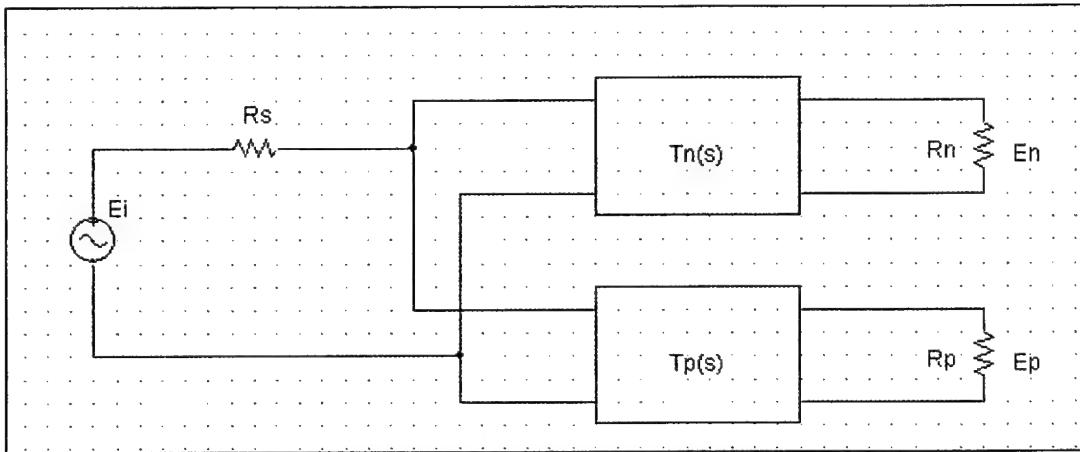


Figure 41. General Structure

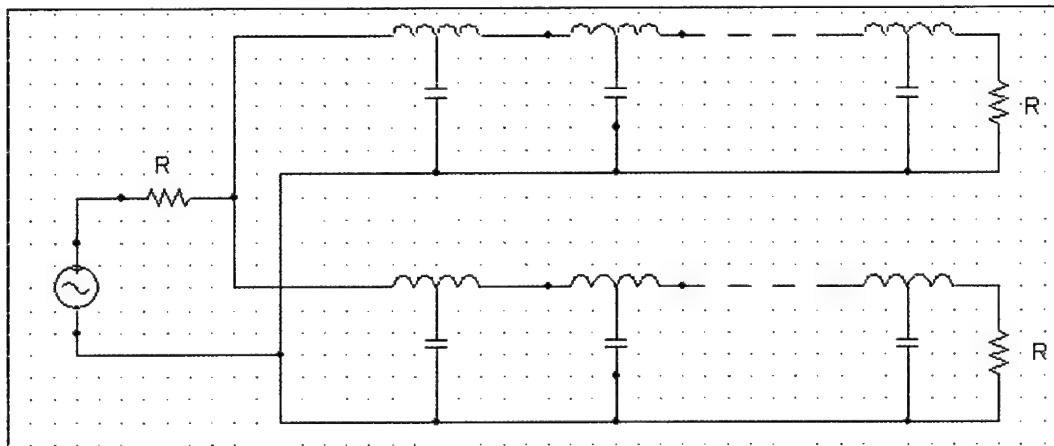


Figure 42. Passive Realization

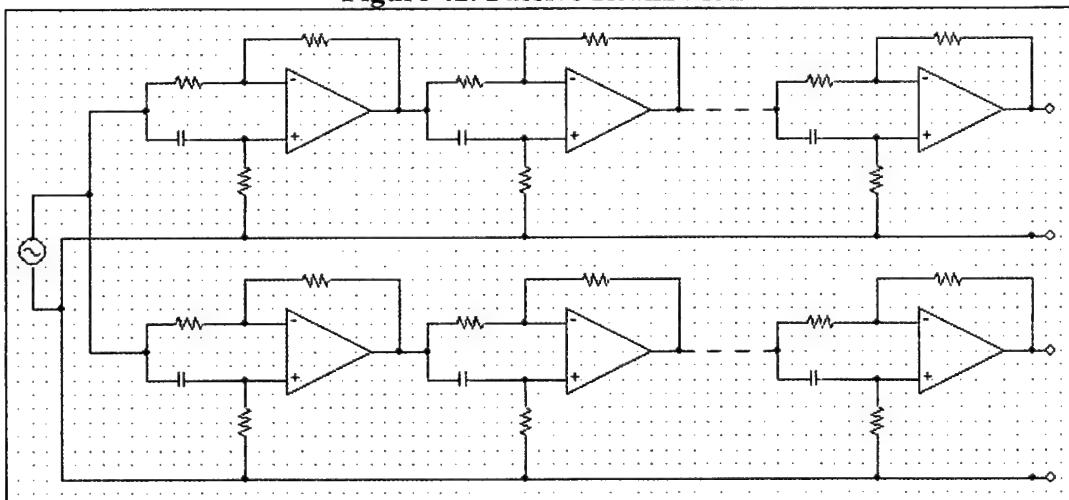


Figure 43. Active Realization

The transfer functions tabulated in Table IV approximate a 90° phase difference in an equi-ripple manner. This approximation occurs within the bandwidth limits ω_L and ω_U as shown in Figure 44. These frequencies are normalized so that $\sqrt{\omega_L \omega_U} = 1$. For a specified bandwidth ratio ω_U/ω_L , the individual band limits can be found from

$$\omega_L = \sqrt{\omega_L / \omega_U} \quad (2.3)$$

$$\omega_U = \sqrt{\omega_U / \omega_L} \quad (2.4)$$

As the total complexity n is made larger, the phase error decreases for a fixed bandwidth ratio, or for a fixed phase error, the bandwidth ratio will increase.

To use Table IV, first determine the required bandwidth ratio from the frequencies given. A network is then selected that has a bandwidth ratio ω_U/ω_L that exceeds the requirement and a phase error $\pm \Delta\phi$ that is acceptable.

Table IV: Pole-Zero Locations for 90° Phase-Shift Networks^[12]

n	$\Delta\phi$	α_N	α_P	ω_U/ω_L
6	6.84°	43.3862	8.3350	1146
		2.0264	0.4935	
		0.1200	0.0231	
8	2.12°	59.7833	14.4159	573.0
		4.8947	1.6986	
		0.5887	0.2043	
		0.0694	0.0167	
10	0.66°	75.8845	20.4679	
		8.3350	3.5631	
		1.5279	0.6545	
		0.2807	0.1200	
		0.0489	0.0132	
6	4.99°	34.3132	7.0607	
		1.9111	0.5233	
		0.1416	0.0291	
8	1.39°	47.0857	11.8249	
		4.3052	1.6253	
		0.6153	0.2323	
		0.0846	0.0212	
n	$\Delta\phi$	α_N	α_P	ω_U/ω_L
10	0.39°	59.6517	16.5238	286.5
		7.06707	3.2112	
		1.4749	0.6780	
		0.3114	0.1416	
		0.0605	0.0168	
4	13.9°	16.8937	2.4258	286.5
		0.4122	0.0592	
6		27.1337	5.9933	

	3.43°	1.8043	0.5542	
		0.1669	0.0369	
8	0.84°	37.0697	9.7136	
		3.7944	1.5566	
		0.6424	0.2636	
		0.1030	0.0270	
10	0.21°	46.8657	13.3518	
		5.9933	2.8993	
		1.4247	0.7019	
		0.3449	0.1669	
		0.0749	0.0213	
4	10.2°	13.5875	2.2308	143.2
n	$\Delta\Phi$	α_N	α_P	ω_U/ω_L
4	10.2°	0.4483	0.0736	143.2
8	0.46°	29.3327	8.0126	
		3.3531	1.4921	
		0.6702	0.2982	
		0.1248	0.0341	
10	0.10°	37.0091	10.8375	
		5.1050	2.6233	
		1.3772	0.7261	
		0.3812	0.1959	
		0.0923	0.0270	
4	7.58°	11.4648	2.0883	81.85
		0.4789	0.0918	
6	1.38°	18.0294	4.5017	
		1.6316	0.6129	
		0.2221	0.0555	
8	0.25°	24.4451	6.8929	
		3.0427	1.4432	
		0.6929	0.3287	
		0.1451	0.0409	
10	0.046°	30.7953	9.2085	81.85
n	$\Delta\Phi$	α_N	α_P	ω_U/ω_L
10	0.046°	4.5017	2.4248	81.85
		1.3409	0.7458	
		0.4124	0.2221	
		0.1086	0.0325	
4	6.06°	10.3270	2.0044	57.30
		0.4989	0.0968	
6	0.99°	16.1516	4.1648	
		1.5873	0.6300	
		0.2401	0.0619	
8		21.8562	6.2817	

	0.16°	2.8648	1.4136	
		0.7074	0.3491	
		0.1592	0.0458	
10	0.026°	27.5087	8.3296	
		4.1648	2.3092	
		1.3189	0.7582	
		0.4331	0.2401	
		0.1201	0.0364	
4	3.57°	8.5203	1.6157	28.65
		0.5387	0.1177	
<i>n</i>	$\Delta\Phi$	α_N	α_P	ω_U/ω_L
6	0.44°	13.1967	3.6059	28.65
		1.5077	0.6633	
		0.2773	0.0758	
8	0.056°	17.7957	5.2924	
		2.5614	1.3599	
		0.7354	0.3904	
		0.1890	0.0562	
10	0.0069°	22.3618	6.9242	
		3.6059	2.1085	
		1.2786	0.7821	
		0.4743	0.2773	
		0.1444	0.0447	
4	1.31°	5.9339	1.5027	11.47
		0.5055	0.1280	
6	0.10°	10.4285	3.0425	
		1.4180	0.7052	
		0.3287	0.0959	
8	0.0075°	14.0087	4.3286	
		2.2432	1.2985	
		0.7701	0.4458	
<i>n</i>	$\Delta\Phi$	α_N	α_P	ω_U/ω_L
8	0.0075°	0.2310	0.0714	11.47

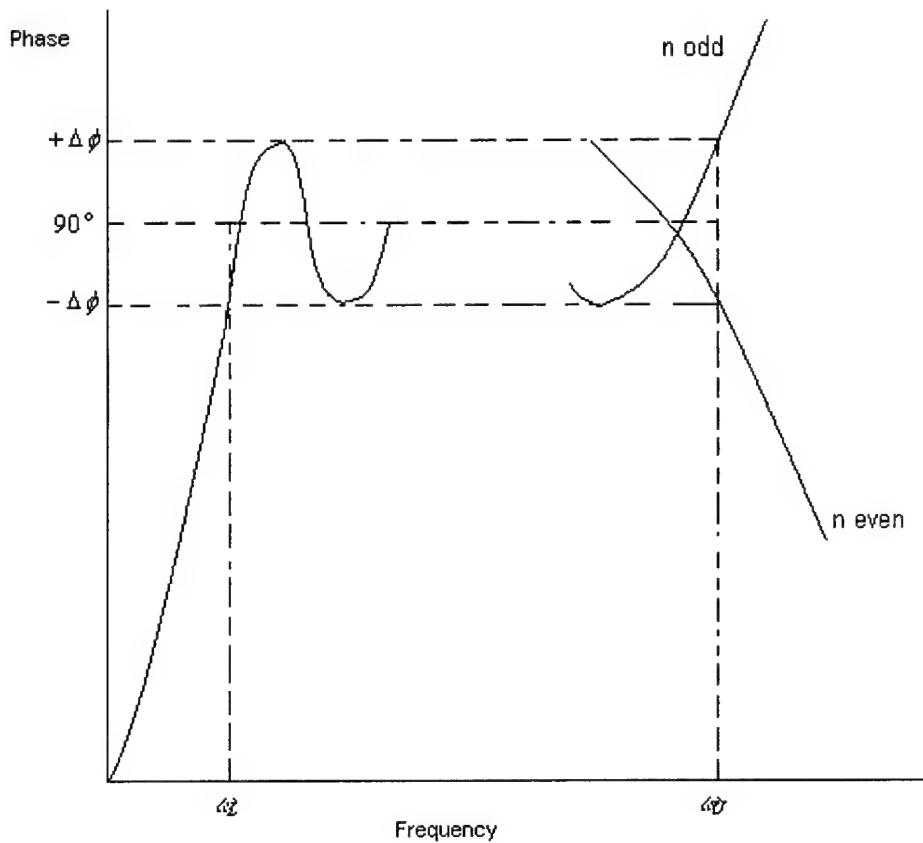


Figure 44. Wide-band 90° Phase-shift Approximation

A frequency-scaling factor (FSF) is determined from

$$FSF = 2\pi f_0 \quad (2.5)$$

where f_0 is the geometric mean of the specified band limits or $\sqrt{f_L f_U}$. The tabulated

α 's are then multiplied by the FSF for denormalization. The resulting pole-zero pairs can be realized by a cascade of active or passive first-order sections for each network.

The 90°-phase shifter that was constructed works from 1 MHz to 6 MHz. The bandwidth ratio required is 6:1. Thus the design corresponding to $n = 6$ and $\omega_U/\omega_L = 11.47$ was chosen from Table IV. The phase-shift error will be $\pm 0.1^\circ$. The normalized pole-zero coordinates for both networks are shown in Table V.

Table V: Normalized Real Pole-Zero Coordinates

<i>P</i> Network	<i>N</i> Network
$\alpha_1 = 10.4285$	$\alpha_4 = 3.0425$
$\alpha_2 = 1.4180$	$\alpha_5 = 0.7052$
$\alpha_3 = 0.3287$	$\alpha_6 = 0.0959$

The frequency-scaling factor (FSF) is

$$FSF = 2\pi f_0 = 2\pi \times 2449489.743 = 15.4 \times 10^6 \quad (2.6)$$

$$\text{Where } f_0 = \sqrt{(1 \times 10^6) \times (6 \times 10^6)} = 2449489.743$$

The pole-zero coordinates are multiplied by the *FSF*, resulting in the set of denormalized values for α shown in Table VI.

Table VI: De-normalized Real Pole-Zero Coordinates

<i>P</i> Network	<i>N</i> Network
$\alpha'_1 = 160.5 \times 10^6$	$\alpha'_4 = 46.83 \times 10^6$
$\alpha'_2 = 21.82 \times 10^6$	$\alpha'_5 = 10.85 \times 10^6$
$\alpha'_3 = 5.06 \times 10^6$	$\alpha'_6 = 1.48 \times 10^6$

The *P* and *N* networks can now be realized using the active third-order all-pass circuit, similar to the one shown in Figure 43. If we let the feedback resistor $R_f = 100 \text{ ohms}$ and $C = 1000 \text{ pF}$, the value of R is given by the following equation.

$$R = \frac{1}{(\alpha_0 \times C)} \quad (2.7)$$

Where the α_0 's are obtained from Table VI. Using the denormalized α 's for the *P* and *N* networks from Table VI the following values as shown in Table VII are obtained.

Table VII: Resistor Values

Section	<i>P</i> Network	<i>N</i> Network
1	$R = 6.23 \Omega$	$R = 21.36 \Omega$
2	$R = 45.82 \Omega$	$R = 92.14 \Omega$
3	$R = 197.67 \Omega$	$R = 677.53 \Omega$

The final circuit is shown in Figure 45 using practical resistor values. The phase shifter is a three stage phase shifter because $n = 6$. The op-amp used is AD8005. The AD8005 was used for several reasons. First, AD8005 is a current feedback operational amplifier, which are inherently very fast operational amplifiers. It is a ultra low power operational amplifier. It only consumes 4 mW of power at a supply voltage of 5 V. Low power consumption is very important because the imaging system is a portable one. The AD8005 also has a low distortion/noise.

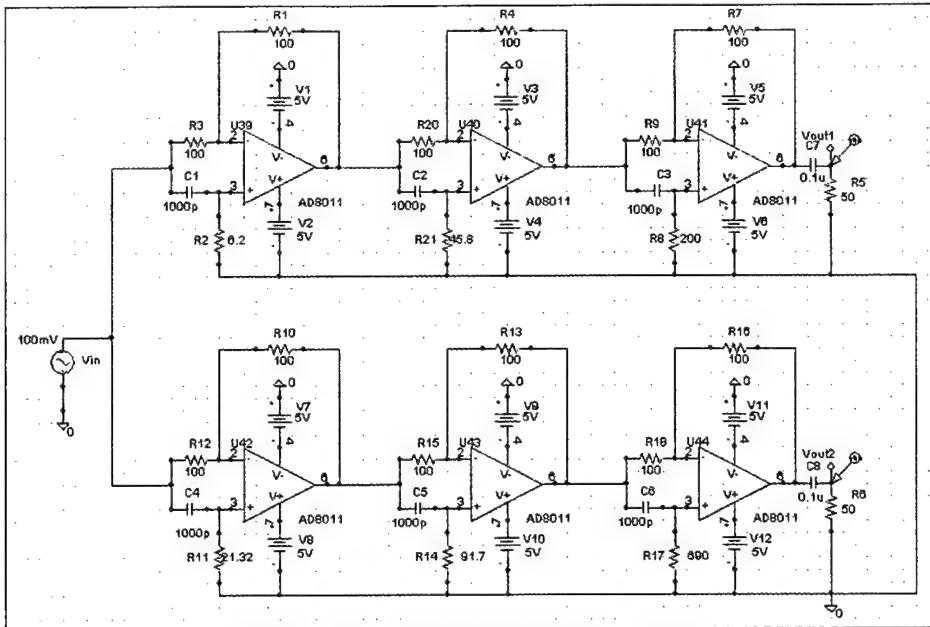


Figure 45. Three-stage Phase Shifter

A two-stage phase shifter, can also be constructed using the same design principles as used above. For the two stage phase shifter $n = 4$ and $\omega_U/\omega_L = 11.47$. As can be seen from Table IV, the phase shift error will be $\pm 1.31^\circ$. The final circuit for two-stage phase shifter is shown in Figure 46. The response of two-stage phase shifter is not as accurate as that of a three-stage phase shifter as can be seen from Table IV.

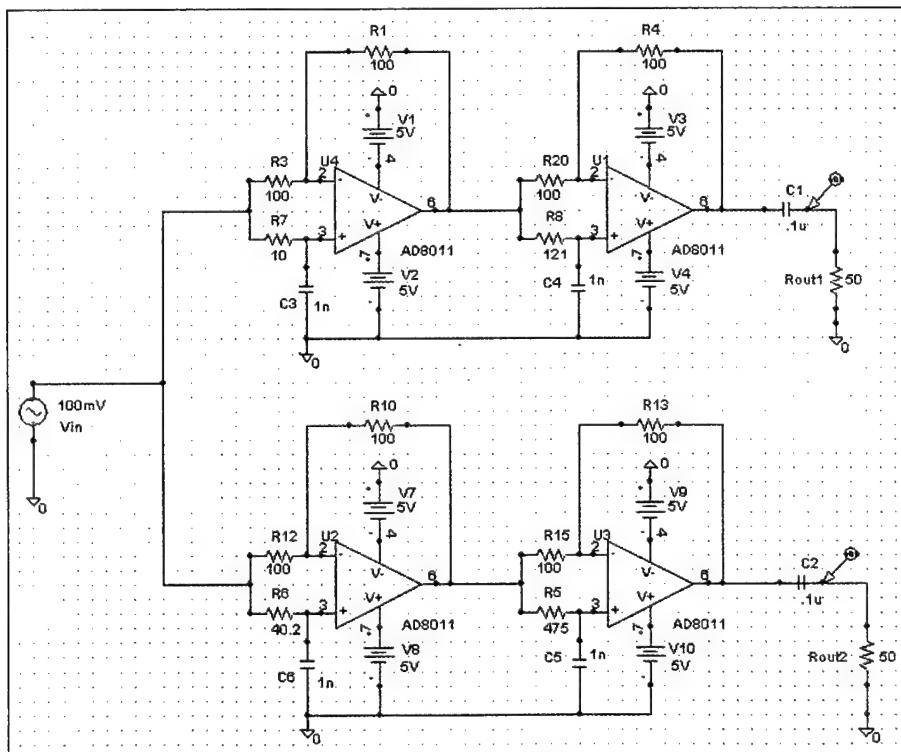


Figure 46. Two-stage Phase Shifter

5.1.4 Differential Amplifier

The differential amplifier is at the front of the phase-shifter. The differential amplifier is needed to add two signals coming out of the doily array, which are 180° of phase, but carry the same information. Figure 47 was used for the differential amplifier.

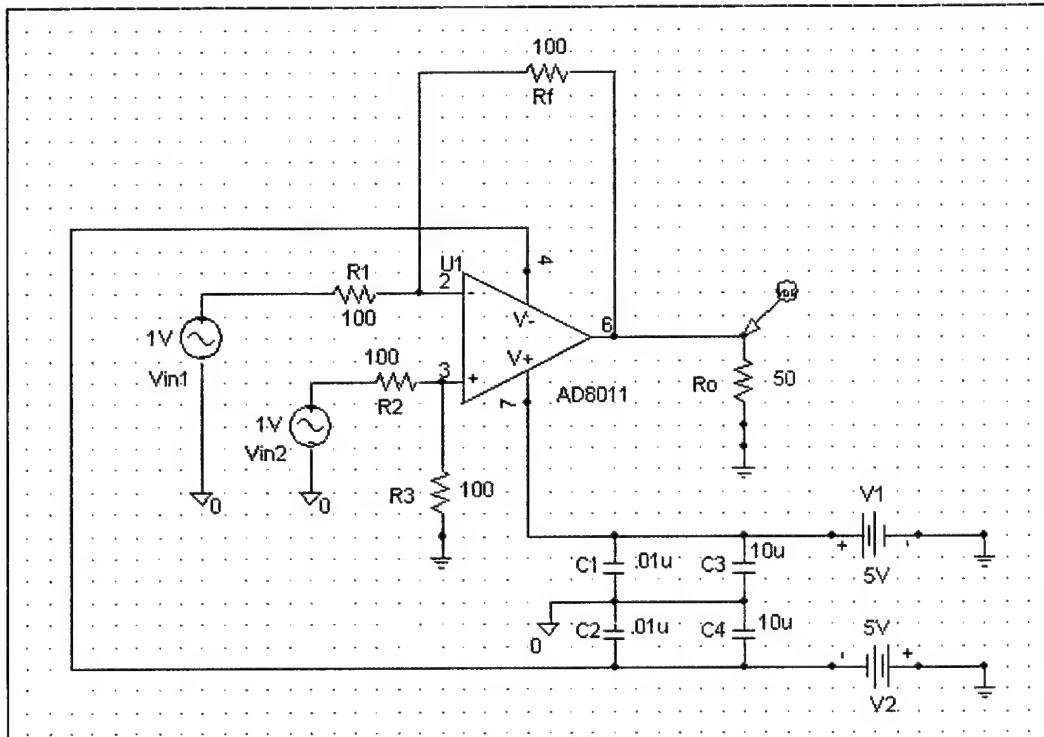


Figure 47. Differential Amplifier

Again, the operational amplifier used was AD8005. Two differential amplifiers were used for each channel of the receiver. The differential amplifier shown above has no gain but the gain can be adjusted as necessary, by changing the feedback resistors. For proper functioning of the receiver it is necessary that the differential amplifier work at a gain of 5. The feedback resistors R_f and R_3 can be changed to 500 at those times.

5.1.5 Output Stage

The output stage of the receiver is configured as a differential output stage. The output stage consists of a summing amplifier with a differential output and a differential amplifier with a differential output stage. Figures 48 and 49 show the output stage.

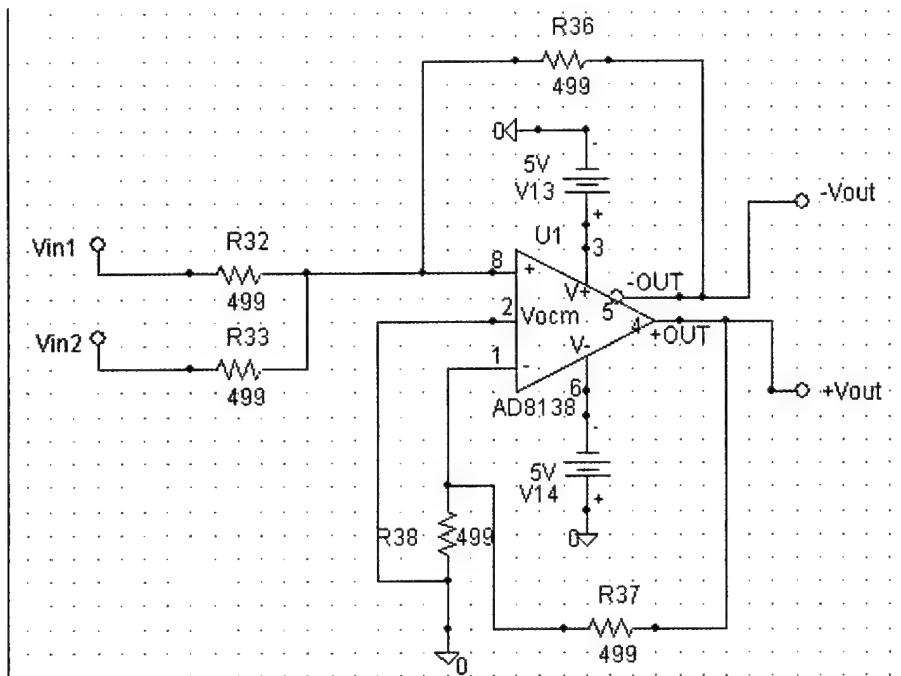


Figure 48. Summer with Differential Output

The operational amplifiers used for the output stage were AD8138. The AD8138 is a major advancement over op amps for differential signal processing. The AD8138 can be used as a single-ended-to-differential amplifier or as a differential-to-differential amplifier. The AD8138 is as easy to use as an op amp, and greatly simplifies differential signal amplification and driving.

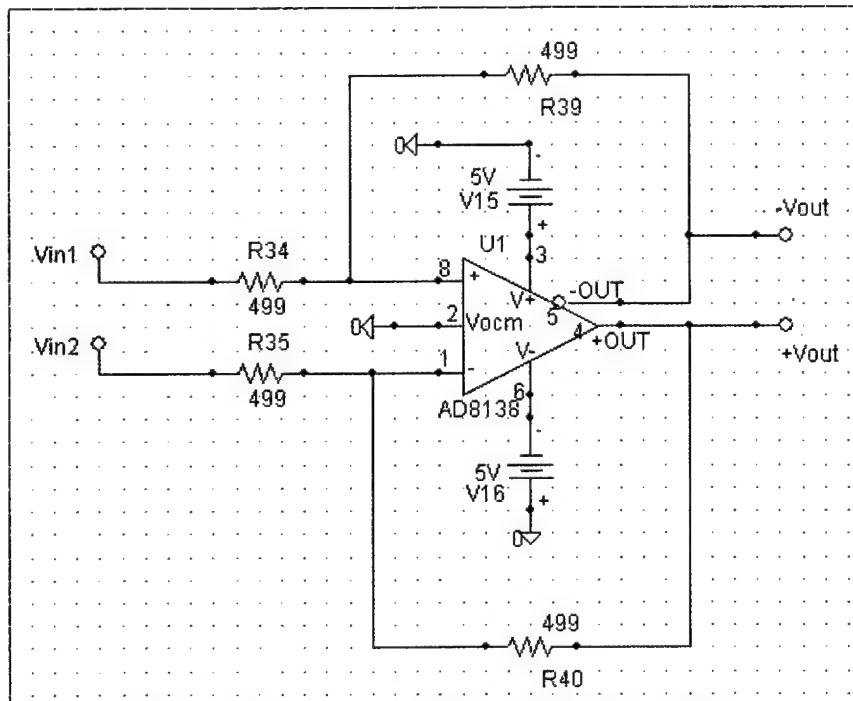


Figure 49. Difference Amplifier with Differential Output

Manufactured on Analog Device's proprietary XFCB bipolar process, the AD8138 has a -3 dB bandwidth of 320 MHz and delivers a differential signal with the lowest harmonic distortion available in a differential amplifier.^[17] The AD8138 has a unique internal feedback feature that provides output gain and phase matching that are balanced, suppressing even order harmonics. The internal feedback circuit also minimizes any gain error that would be associated with the mismatches in the external gain setting resistors.

The AD8138's differential output helps balance the input-to-differential ADCs, maximizing the performance of the ADC. The AD8138 eliminates the need for a transformer with high performance ADCs, preserving the low frequency and dc information. The common-mode level of the differential output is adjustable by a voltage on the VOCM pin, easily level-shifting the input signals for driving single supply ADCs. Fast overload recovery preserves sampling accuracy.

The AD8138 distortion performance makes it an ideal ADC driver for communication systems, with distortion performance good enough to drive state-of-the-art 10- to 16-bit converters at high frequencies. The AD8138 offset and dynamic performance make it well suited for a wide variety of signal processing and data acquisition applications. To summarize AD 8138 has the following features.

Features

- Easy to Use Single-Ended-to-Differential Conversion
- Adjustable Output Common-Mode Voltage
- Externally Adjustable Gain
- Low Harmonic Distortion
 - 94 dBc-Second, –114 dBc-Third @ 5 MHz into 800 Ω Load
 - 87 dBc-Second, –85 dBc-Third @ 20 MHz into 800 Ω Load
 - 3 dB Bandwidth of 320 MHz, G = +1
- Fast Settling to 0.01% of 16 ns
- Slew Rate 1150 V/ms
- Fast Overdrive Recovery of 4 ns
- Low Input Voltage Noise of 5 nV/ $\sqrt{\text{Hz}}$
 - 1 mV Typical Offset Voltage
 - Wide Supply Range +3 V to 65 V
 - Low Power 90 mW on +5 V
 - 0.1 dB Gain Flatness to 40 MHz
 - Available in 8-Lead SOIC

The AD8138 differs from conventional op amps in that it has two outputs whose voltages move in opposite directions. Like an op amp, it relies on high open loop gain and negative feedback to force these outputs to the desired voltages. The AD8138 behaves much like a standard voltage feedback op amp and makes it easy to perform single-ended-to-differential conversion, common-mode level shifting, and amplification of differential signals. Also like an op amp, the AD8138 has high input impedance and low output impedance. Previous differential drivers, both discrete and integrated designs, have been based on using two independent amplifiers, and two independent feedback

loops, one to control each of the outputs. When these circuits are driven from a single-ended source, the resulting outputs are typically not well balanced. Achieving a balanced output has typically required exceptional matching of the amplifiers and feedback networks.

DC common-mode level shifting has also been difficult with previous differential drivers. Level shifting has required the use of a third amplifier and feedback loop to control the output common-mode level. Sometimes the third amplifier has also been used to attempt to correct an inherently unbalanced circuit. Excellent performance over a wide frequency range has proven difficult with this approach. The AD8138 uses two feedback loops to separately control the differential and common-mode output voltages. The differential feedback, set with external resistors, controls only the differential output voltage. The common-mode feedback controls only the common-mode output voltage. This architecture makes it easy to arbitrarily set the output common-mode level. It is forced, by internal common-mode feedback, to be equal to the voltage applied to the VOCM input, without affecting the differential output voltage.

The AD8138 architecture results in outputs that are very highly balanced over a wide frequency range without requiring tightly matched external components. The common-mode feedback loop forces the signal component of the output common-mode voltage to be zeroed. The result is nearly perfectly balanced differential outputs, of identical amplitude and exactly 180 degrees apart in phase.

5.2 PSPICE Modeling

The whole receiver and each of the modules where first modeled in PSPICE and tested. The design performance was simulated using MicroSIM DesignLab SPICE software package.^[19] The circuit gave desired output when it was tested. The modules that where simulated in PSICE were the Redwood transducer model, the preamplifier, the differential amplifier, the phase shifter, and the whole system together. All of the above testing was done on a current feedback amplifier. The current feedback amplifier used was AD8011 instead of AD8005, as the model of AD8005 is not available.^[29] Both, AD8011 and AD8005 are current feedback amplifiers and both of them have very similar characteristics.^[18]

5.2.1 Redwood Model

The Redwood model consists of an electrical equivalent circuit for the transducer shown in Figure 50. The Redwood model for a transducer gives the same response when fired, as the actual transducer would give.

Figure 51 shows the response of the circuit when simulated in PSPICE. The y-axis represents the amplitude in dB, while the x-axis represents the frequency. The plot above is from 1-6 MHz.

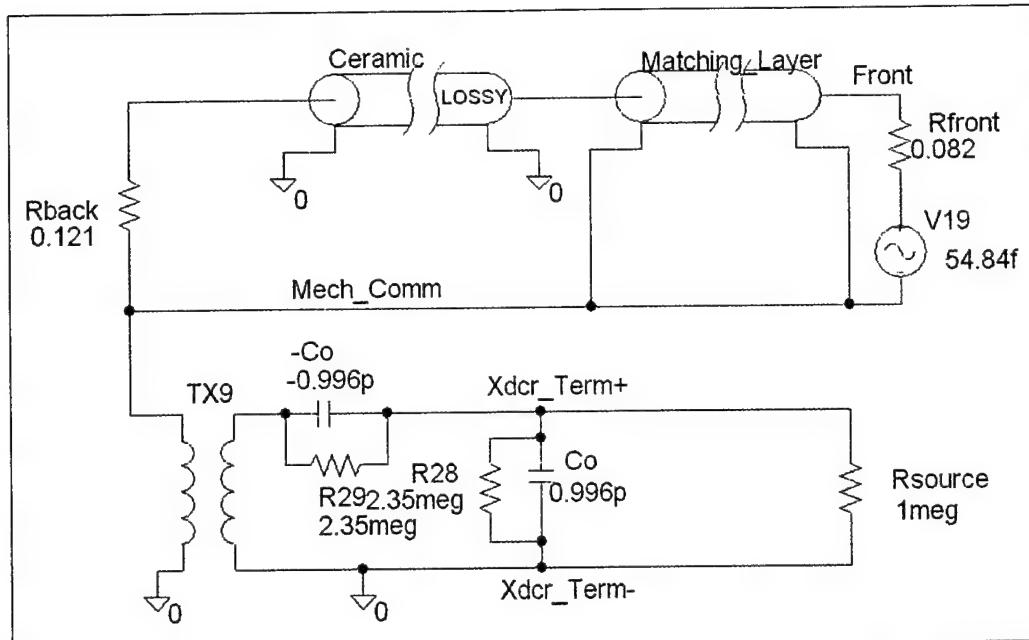


Figure 50. Redwood Model of the Transducer

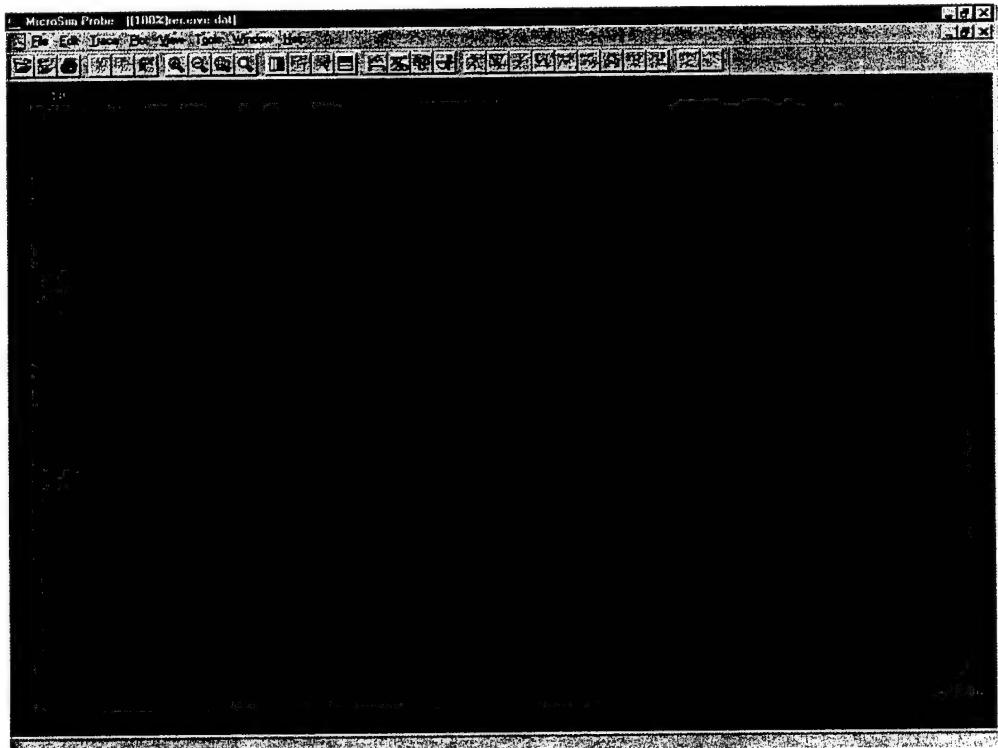


Figure 51. Transducer Predicted Transmit Response

5.2.2 Preamplifier

The preamplifier that was simulated is as shown in Figure 52.

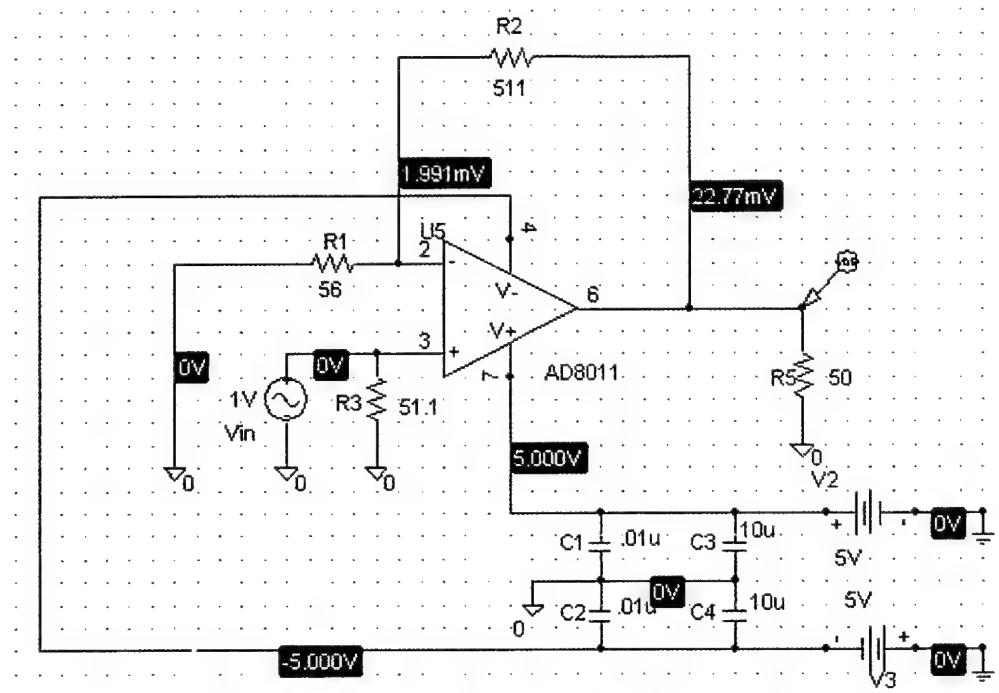


Figure 52. P-Spice Model of the Pre-amplifier

As mentioned previously, the operational amplifier used for simulation was AD 8011 that is a current feedback operational amplifier. The simulation was done from 1KHz to 10 MHz and both the frequency gain response and the phase response were obtained. The frequency response is as shown in Figure 53. As can be seen from the figure the frequency gain response is around 20 dB (which is as expected, because the preamplifier above has a gain of 10) from 1KHz to 10 MHz.



Figure 53. Preamplifier Frequency Response

Figure 54 the preamplifier phase response from 1KHz to 10 MHz. As can be seen it's around zero degrees in the entire range. Thus the preamplifier introduces no additional phase shift in the circuit.

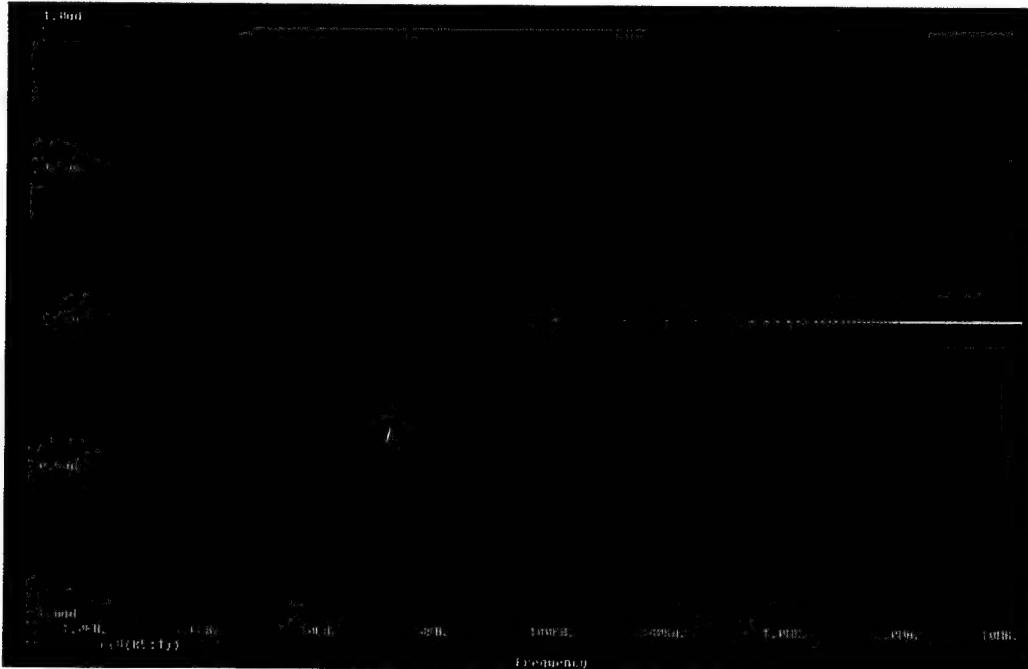


Figure 54. Pre-amplifier Phase Response

5.2.3 Differential Amplifier

The schematic of the differential amplifier is as shown below in Figure 55.

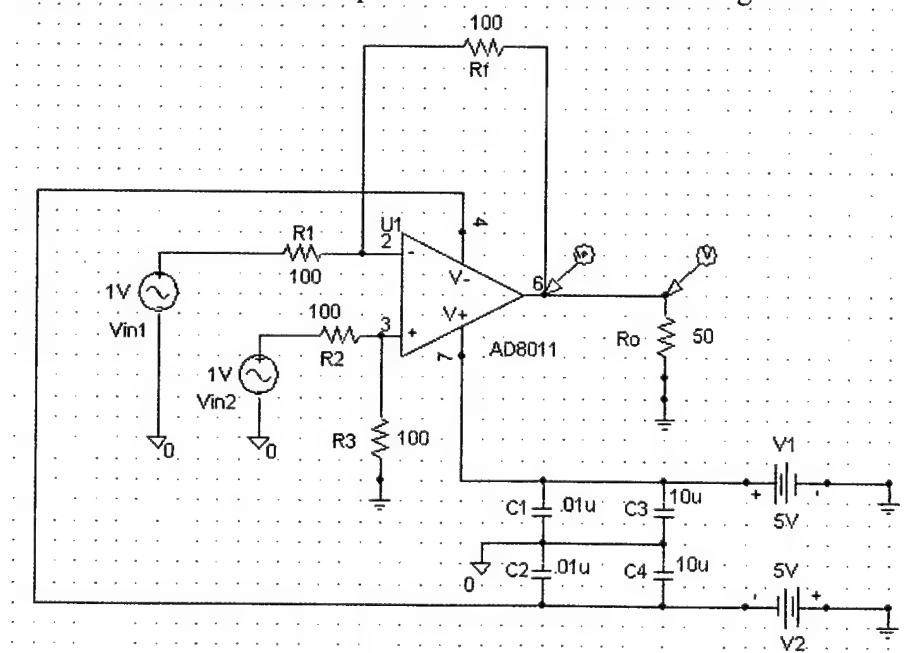


Figure 55. Differential Amplifier Circuit

The differential amplifier as shown above doesn't have a gain. The gain can be modified by changing the feedback resistors. As mentioned previously, the amplifier used for simulation in PSPICE was AD 8011. The plots for the above circuit are as shown in Figure 56. In the plot below the red line is the amplitude while the green line is the phase. The plots are from 1 MHz to 6 MHz. The plot is flat for both the phase and amplitude as required.

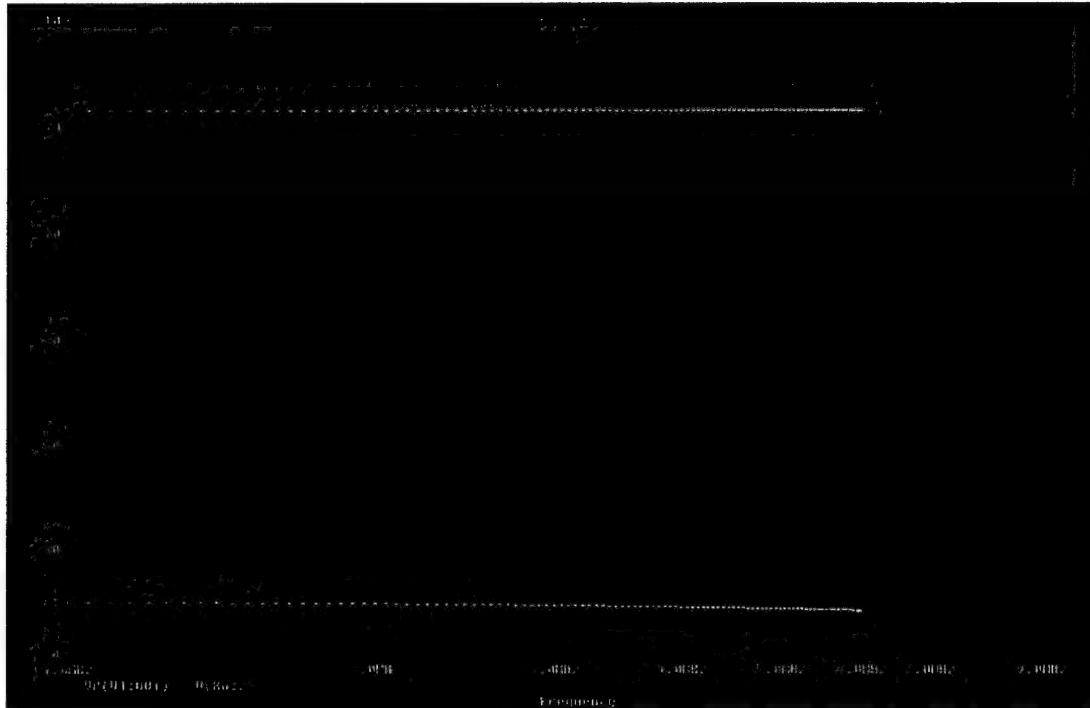


Figure 56. Differential Amplifier Plot

5.2.4 Phase Shifter

Both the three-stage and the two-stage phase shifters were simulated. The three stage and two stage phase shifters are shown in Figure 45 and Figure 46 respectively. The response of the three-stage phase shifter is as shown in Figures 57 and 58. As can be seen from Figure 57, the amplitude changes by less than 0.1 dB over the band (1 MHz-6 MHz). Also the phase changes by less than one degree over the band. The response of a two-stage phase shifter is shown in Figure 59 and 60. As can be seen from Figure 58 the amplitude response changes by less than 0.1 dB over the band. However the phase changes by around four degrees over the band, as can be expected from the theory. As a result three-stage phase shifter was implemented.

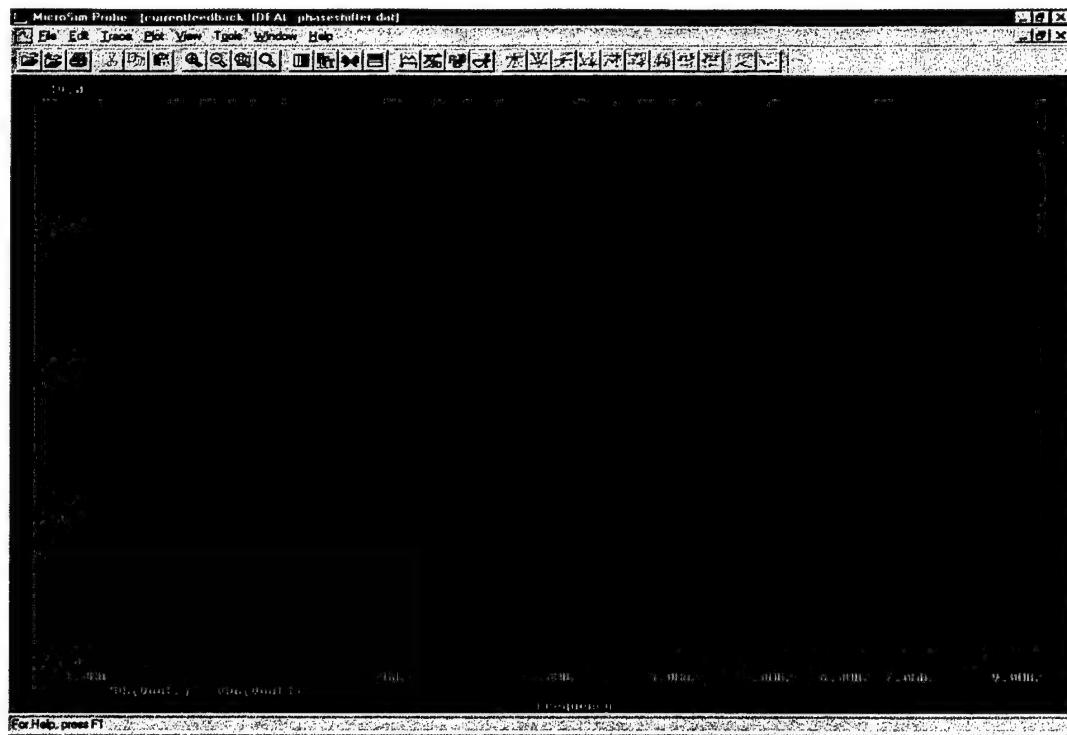


Figure 57. Three-stage Phase Shifter Amplitude Response



Figure 58. Three-stage Phase Shifter Phase Response

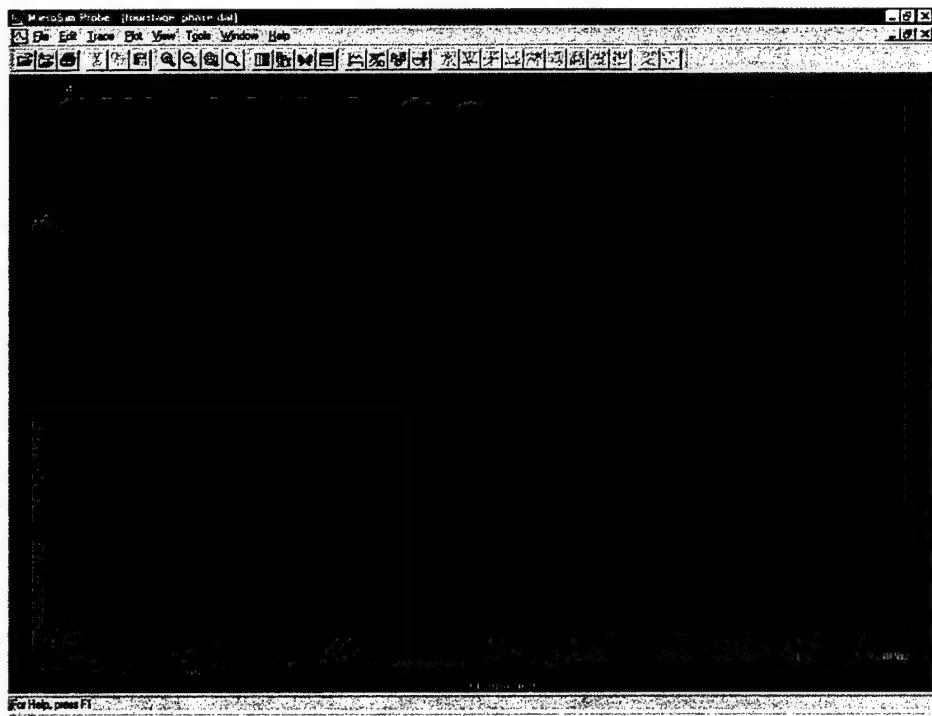


Figure 59. Two-stage Phase Shifter Amplitude Response



Figure 60. Two-stage Phase Shifter Phase Response

5.2.5 The Whole System

The receiver as shown in Figure 35 was also simulated in PSPICE. Figure 61 shows the response when it was simulated.

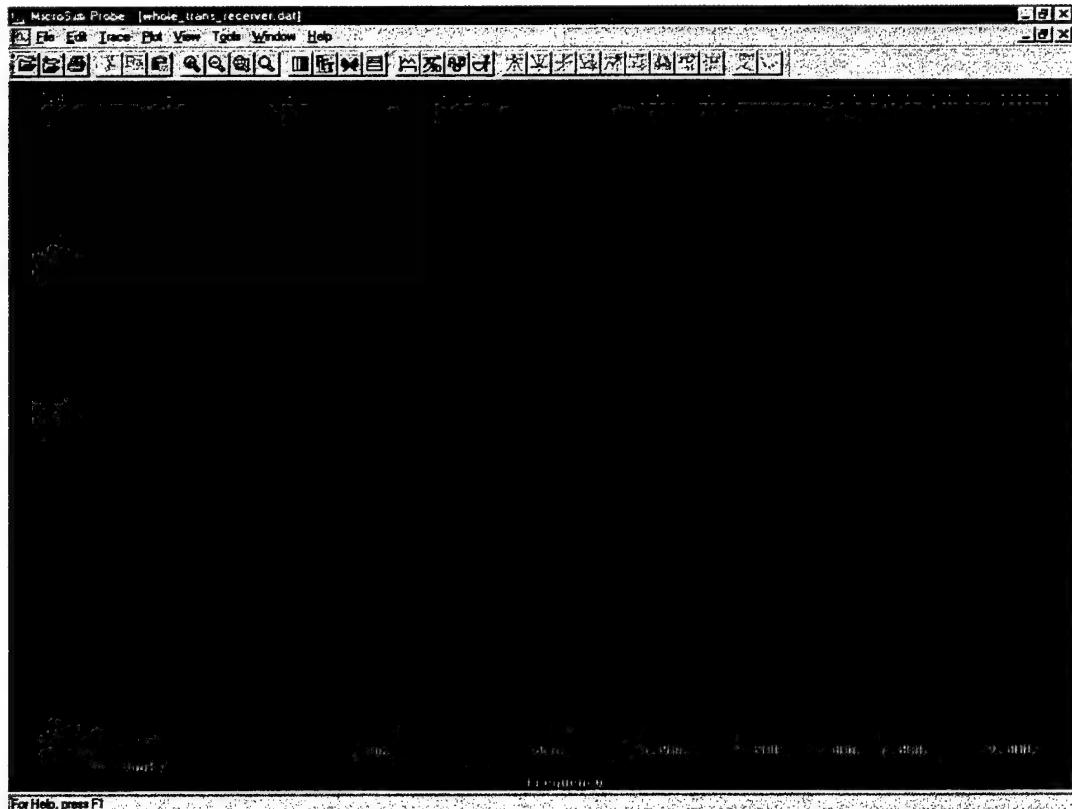


Figure 61. Frequency Response of Receiver

The reason the whole receiver was simulated was to see the frequency response when all the modules are integrated in the system. As can be seen from Figure 60 the amplitude changes by less than 0.3 dB from 1 MHz to 6 MHz. Thus all of the modules function well together when simulated. The next chapter discusses the design of the PCB boards.

6.0 PCB DESIGN

In this Chapter, the following topics are discussed:

- Brass Board Layout
- PCB Design Techniques
- PCB Design

6.1 Brass Board Layout

Each of the modules of the entire circuit was first laid down on a brass board and tested. Surfboards were used to lay down the chips on the board.

The surfboards shown in Figure 62 are for 8 pin SOIC package chips. The operational amplifiers were placed on these surfboards.

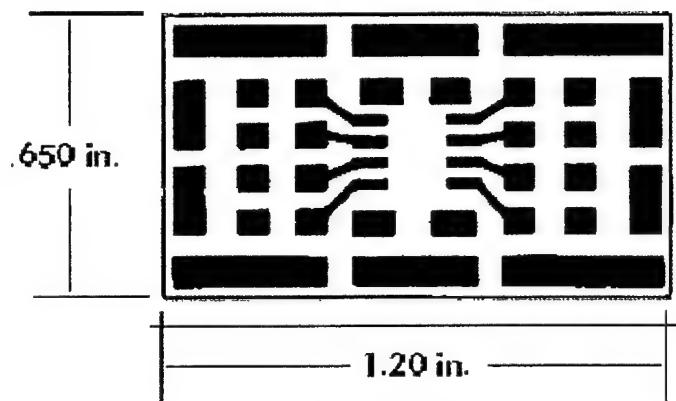


Figure 62. Surfboards

The response of the phase-shifter was not 90 degrees throughout the band, at first, when the surfboards were not used. This problem was later solved when the resistor values used in the phase-shifter were scaled down from 10K to 100 ohms. This reduced the Miller capacitance on the inverting input of the current feedback op-amp (AD8005). Also the path lengths were greatly reduced by placing the op-amps on surfboards. The plots obtained after this gave a phase difference of 90 degrees across the band with an error of + or - 2 degrees. The plots are shown in Chapter 4.

Initially only the AD8005 was laid on this surfboards, and all the remaining components were laid on the brass board. These greatly increased the path length. These led to lot of parasitic capacitance in the circuit, which in turn led to a bad response and the circuit was not working as expected. Later on, all the components used were surface mounted and all of them were laid on the surfboard itself. These led to very small path lengths and the performance of the circuit greatly improved. The whole receiver was laid down on a brass board using the surfboards above and tested. The circuit performed as expected.

6.2 PCB Design Techniques

Several issues related to PCB design techniques for complex high frequency systems are discussed in the following sub-sections.

6.2.1 Electromagnetic Compliance

The design of PCBs for high frequency signals requires a need to follow the correct techniques for Electromagnetic Compliance. Electromagnetic Compliance (EMC) is defined as:

"The ability of a product to coexist in its intended electromagnetic environment without causing or suffering functional degradation or damage."

The major aspects of EMC are:

1. **Emissions** Radiation and propagation of EMI from non-compliant devices in radio frequencies
2. **Susceptibility** Effect of EMI on susceptible devices in form of electrostatic discharge and electrical overstress

Radio Frequencies are defined as the frequency range from 10 kHz to 100 GHz where coherent electromagnetic radiation is useful for communication purposes. RF electromagnetic radiation could be intentional or unintentional. As explained above, unintentional radiation may cause electrical overstress or electrostatic discharge. Electrical Overstress is defined as the damage or loss of functionality experienced by an electronic device due to high voltage pulse. Electrostatic Discharge can be defined as a high voltage pulse, which can cause electrical overstress. This includes events of lesser charge initiated by human beings and also high charge lightning events.

6.2.2 EMC Considerations for PCBs

The cause of Electromagnetic Interference (EMI) on a Printed Circuit Board has no exact mathematical explanation. Since there are many known and unknown variables associated with the EMI on a PCB working at higher frequencies, it is not possible to guarantee any design for EMC. One of the primary reasons for EMI is the behavior of passive devices at high frequencies. Figure 63 shows the approximate equivalent model of passive devices at low and high frequencies.

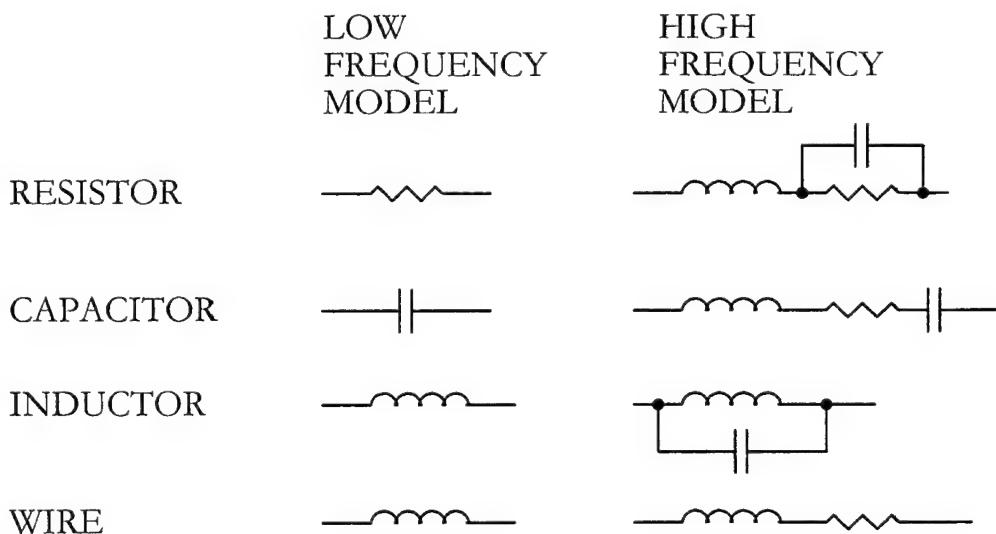


Figure 63. Low and High Frequency Model for Passive Components

As seen in Figure 63, the impedance behavior of passive components is not the same at low and high frequencies. This variation of behavior with frequency is also referred as hidden schematic. This hidden behavior introduces extra components in the circuitry at high frequency, which might cause resonance. Many times, the cause of EMI is the lack

of consideration of the frequency response in a high frequency design. Both time domain and frequency domain analysis should be carried out properly. If these hidden components are considered carefully in the design, it is easier to avoid EMI. Again, these are just approximate models for high frequency behavior so considering them in the design only reduces the chances of EMI.

For EMI to exist in a design, the following components must co-exist.

1. Source of Energy
2. A susceptible device which acts as a receptor
3. Path between the source and the receptor

Absence or removal of any of these components can remove EMI from design. To make the design electromagnetic compatible, an effort should be made to reduce the possibility of existence of any of these components. It is hard to realize the coupling path between the source and a receptor on a large and complex mixed signal high frequency system. After careful considerations of various design issues, if the EMI does exist, the first effort should be directed to find the receptor, which is closing the feedback loop. This can be done by analyzing the frequency spectrum by adding a small amount of impedance at obvious susceptible nodes in the design. Once the receptor is found, the efforts should be directed to find the coupling path. In a complex system, there can be more than one sources, which might be causing the radiation. If the coupling path is found, one should try to remove that path by component readjustment and if necessary, by redesigning the layout.

6.2.3 Layer Stack Guidelines

The Layer Stack order is also an equally important design issue as is the electromagnetic compliance. The order should be such that each and every signal layer is adjacent to at least one plane layer. Also the number of layers on a board is an equally critical decision and is more application driven.

Two layer boards are generally used for low frequency analog designs. The power and ground traces should be placed on separate layers. The total length of power traces should be kept to a minimum. The ground traces should be routed parallel to each other and also close to the signal traces. This would help in minimizing the loop currents created by high frequency switching noise. Ground loops are one of the primary reasons for RF noise. RF noise is produced when the physical distance between multi-point grounds is significant. A ground loop consists of a part of signal path and part of the ground plane. A ground loop is created when two circuits are connected to the main ground reference (chassis) by multi point ground techniques. A difference in ground reference exists between these two points due to the finite impedance between the two points. This might inject the noise from one circuit to the other circuit.^[20]

Three layer boards are rarely used. The top layer should be used for signal while the bottom should be used for the power. In this stack order, the signal layer would exhibit excellent RF current flux cancellation and also good noise margins. But such a stack is limited to designs with very simple routing. Four layer boards are used in high frequency analog system with moderate complexity of routing. The top and bottom layers are used

for routing. The inner two layers are used for power and ground separately. Continuous power and ground plane help in EMI suppression. Figure 64 shows the stack for the four layer boards.

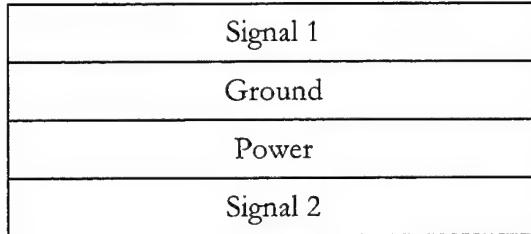


Figure 64. Layer Stack for 4 Layer Boards

One of the signal layers adjacent to the power plane will exhibit poor flux cancellation of RF currents compared to the one, which is adjacent to the ground plane. The reason for this poor cancellation is due to the asymmetrical pull-up and pull-down current ratios of a device. This causes an imbalance in the power and ground plane structure. Power planes, due to this flux phase shift, do not perform good RF current flux cancellation compared to ground plane.

6.2.4 Grounding Methods

Grounding can be done in either of the two basic choices: Single Point and Multi Point. Single point grounding is used when the application is limited to 1MHz or below frequencies. In single point grounding, all the grounds meet at one point on a PCB or all the grounds are connected in series and grounded at one point. This technique is usually used for analog instruments, audio circuits and dc power instruments.

The impedance of the trace and the plane increases with frequency and at high frequencies it can not be neglected. These traces can act as an antenna and start to radiate RF energy. Multi point grounding shunts the RF currents on the ground planes and minimizes the impedance. At higher frequencies, even a small increase in the length of the ground path can be critical. All component leads and the traces going to ground should be kept to a minimum. The traces introduce unseen inductors in the circuitry. These inductors when combined with the plane capacitance can cause resonance in the circuit. Multi point grounding would put all the traces going to ground, in parallel at high frequencies. This would help to lower the impedance and thereby reduce the chances of EMI.

6.2.5 Bypassing and Decoupling

Bypassing and decoupling helps to reduce the unwanted energy transfer between devices. Decoupling removes the RF energy generated on the power planes by the high frequency components. These capacitors also provide a localized source of dc power and reduce the peak current surge propagation. Bypassing removes unwanted RF noise that couples

component or cable EMI. It also provides filtering. When a multi layer board is used for high frequency applications, adjacent placement of power and ground planes act as a one large decoupling capacitor. This provides decoupling for low frequency components. The next section discusses the design of the PCBs based on the above principles.

6.3 One Channel PCB

The op-amp used was AD8005. The circuit was first laid on the copper board and analyzed. Figure 65 shows the layout of one channel phase shifter in OrCAD.^[24]

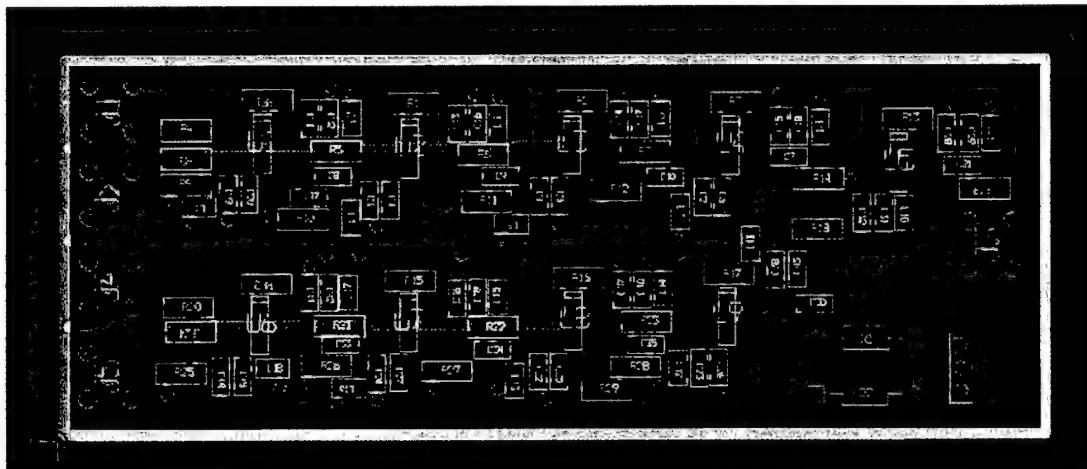


Figure 65. One Channel PCB

Layers: 4

TOP: Signal

BOTTOM: Signal

POWER PLANE: +5 volts, -5 volts

GROUND PLANE: Analog Ground

The above PCB consists of the phase shifter and the summer. The above PCB uses SMA connectors for testing purposes. For a four-layer board the components can be laid on both sides, the components were laid only the topside for the above design. This reduced the complexity of the circuit. Components were mounted on the above PCB and it was tested. The results are shown in Chapter 4.

6.3.1 Power Plane Design

This design requires only two power levels, +5 and -5 volts. This makes the power plane design simple for this board. The power plane is shown in Figure 66.

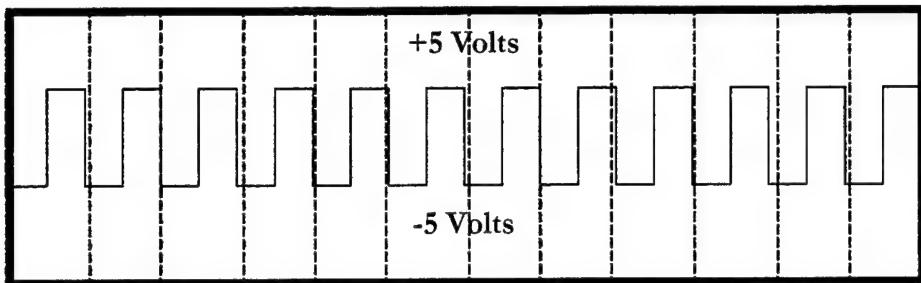


Figure 66. Power Plane

As seen in the Figure 66, the power plane is "comb" shaped. On one side the voltage level is +5 volt while on the other side it is -5 volts. The comb is laid out such that power levels between the channels are not continuous. This can be further explained using Figure 67.

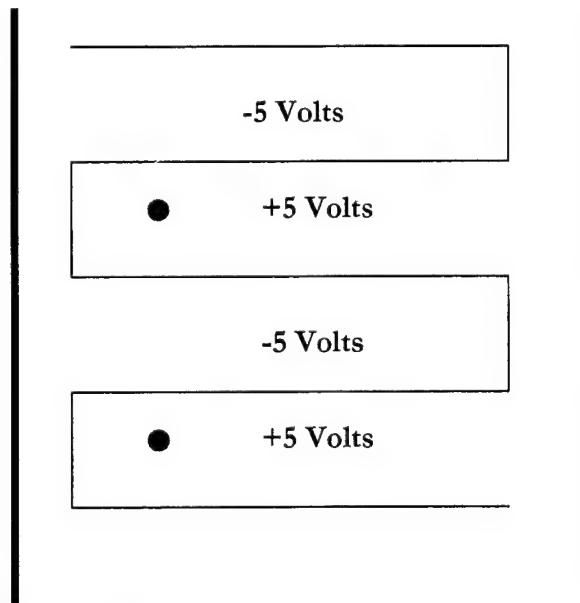


Figure 67. Power Plane Isolations

As seen in the Figure 67, the two black dots are electrically connected but magnetically isolated. The flux lines emerging from each point cannot get coupled with the lines emerging from adjacent channel due to discontinuity. This design reduces the EMI susceptibility of the board.

6.3.2 Ground Plane Design

Figure 68 shows the ground plane design. The ground plane is designed such that it is electrically continuous, but it is discontinuous for the magnetic flux lines in between each individual leg of the phase shifter. This can be further explained by Figure 69.

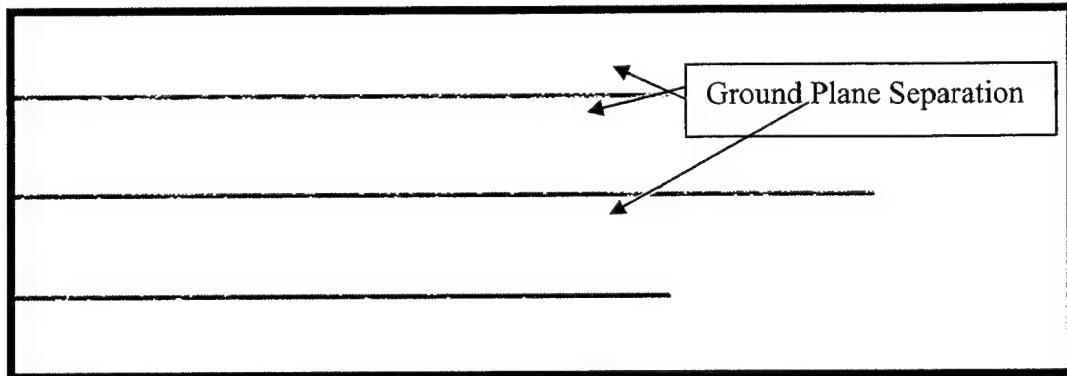


Figure 68. Ground Plane Design

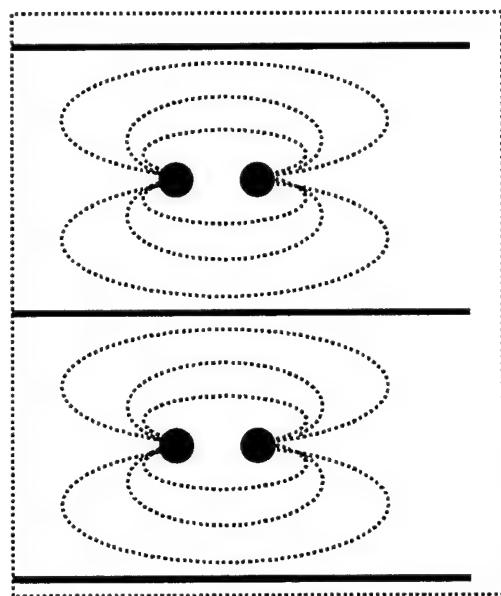


Figure 69. Ground Separation

As seen in Figure 69, the plane is continuous at the right hand side but it is separated between each channel. This stops the magnetic flux lines and ground currents of one leg to couple with the ground currents of the adjacent legs. Therefore, the continuity of ground plane remains intact within each leg and inter leg decoupling is achieved. Thus basically the ground currents from one leg are prevented from flowing into the other leg, thus reducing the path length of the current flow.

6.4 Multi Channel PCB

The design for the one channel PCB was later extended to an eight channel PCB. There were two distinct approaches considered for the eight channels PCB. The first approach consisted of designing the eight-channel PCB, just by extending the design of one channel PCB. This approach consisted of designing all the eight channels on the same

PCB board, with common ground and power supply. The next approach consisted of designing each individual channel (called daughter boards from now on), similar to the one discussed in Section 3.3 and then mounting them on board called the motherboard. The input/output connectors, ground and the power supply connectors would reside on the motherboard. Both of them are discussed below.

6.5 Eight Channel Receiver

As mentioned previously, the eight-channel receiver was designed in ORCAD, and is shown in Figure 70. The following diagram shows the layout of the eight-channel PCB with SMA connectors. The board specifications are as follows.

Layers: 4

TOP: Signal

BOTTOM: Signal

POWER PLANE: +5 volts, -5 volts

GROUND PLANE: Analog Ground

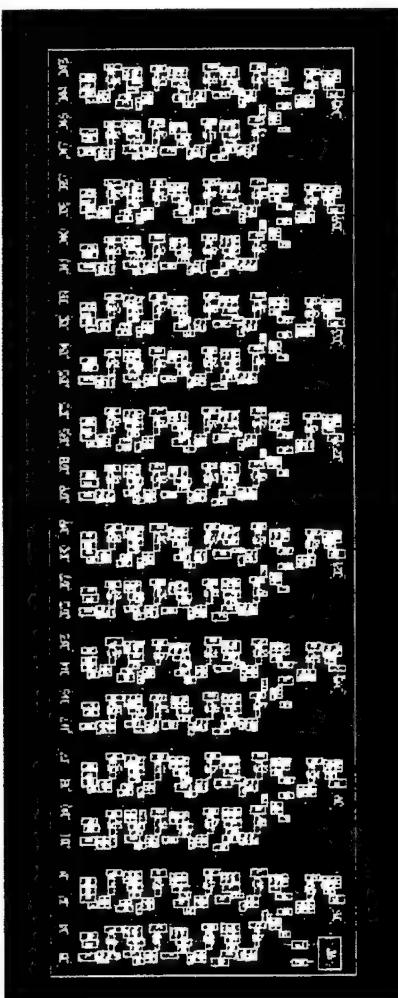


Figure 70. Eight-channel Receiver with SMA Connectors

6.5.1 Power Plane Design

The design involves only two power levels, +5 and -5 volts. The power plane design is as shown in Figure 71. As shown in the figure, the area enclosed by a comb shaped structure is +5 V. Everything else in the power plane on the board is -5 V. Thus the power plane is divided into two distinct areas. One of the areas, which is enclosed is +5 V. The other area, which is simply rest of the board is -5 V. The green line as can be seen in Figure 70 provided the insulation between these two layers.

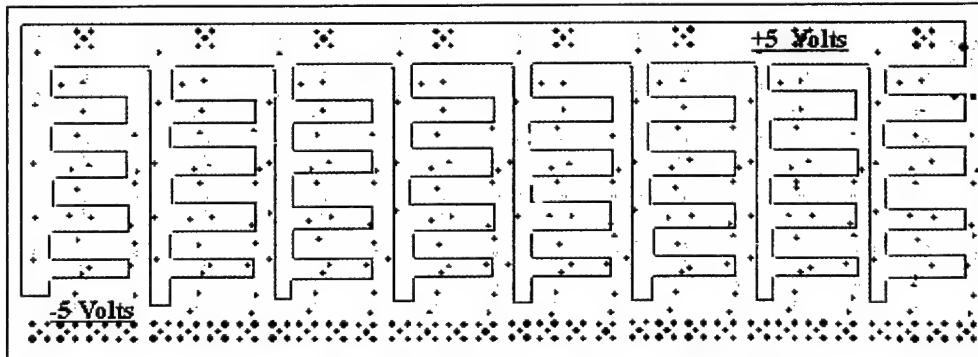


Figure 71. Eight-channel Power Plane Design

6.5.2 Ground Plane Design

Figure 72 shows the ground plane design.

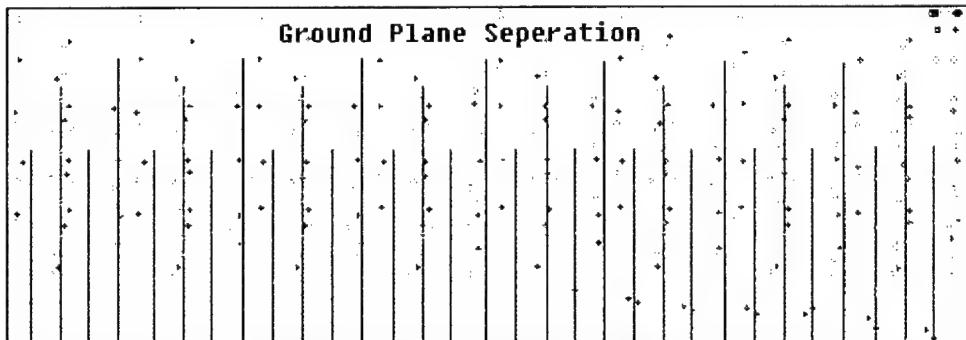


Figure 72. Eight-channel Ground Plane Design

The gray lines in Figure 72, shows the ground plane separations between the channels and also within the channels. This design is a natural extension of the design on ground plane of one channel receiver that is explained in Section 3.3.2. Thus this design follows the same principles as discussed in Section 3.3.2.

In each channel, the design of eight-channel receiver, is same as it was for the single channel design. So the same characteristics are achieved for each channel even when they are put in this fashion.

Later on, AMP connectors will replace the SMA connectors for the input and the output. Figure 73 shows the modified design with the AMP connectors. The ground plane and the power plane for this design is the same as that discussed for the eight-channel

receiver above. As mentioned, the AMP connectors replaced the SMA connectors. AMP part number 767039-1 was the connector used for input, while AMP part number 767089-1 was the connector used for output. Both of them are controlled impedance connectors. A discussion about the two follows.

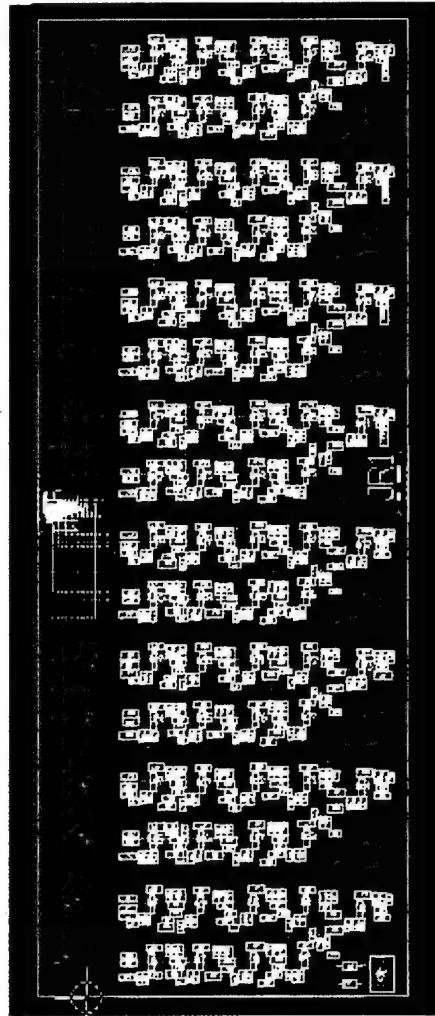


Figure 73. Eight-channel Receiver with AMP Connectors

6.5.3 AMP Connectors

The AMP connectors used were MICTOR.^[25] The AMP MICTOR connectors are used in all industries where high-speed signal integrity is needed and are surface mount 0.5mm, micro-strip designed connectors.

Figure 74 shows several different MICTOR models. The MICTOR connector is a controlled impedance connector due to the ground blade present between the two signal rows. These surface mount connectors can be used for parallel, right angle, or coplanar board-to-board configurations.^[26]

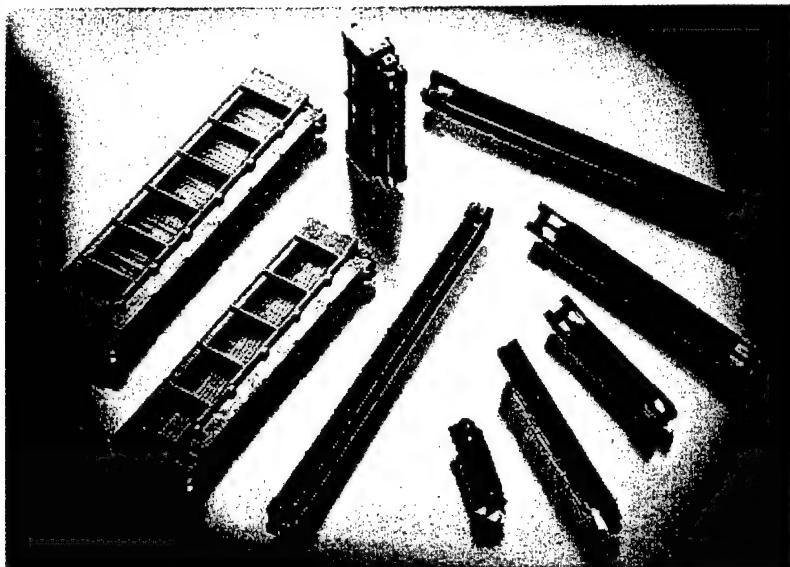


Figure 74. AMP MICTOR Family of Connectors

Various mated heights are available for parallel board-to-board systems. Custom stacking heights can be provided. The MICTOR connector family is available in .025" [.64mm] centerlines in increments of 38 signal positions up to 266 positions. There is a discrete ground bus every $\frac{1}{2}$ inch of the connector length. For more information on the MICTOR family of connectors, refer AMP catalog #65194. The MICTOR connector family is based on the micro-strip concept of two rows of signal contacts divided by a center power ground plane. MICTOR connectors are motherboard and daughter board compatible and include designs for cable-to-board applications. Redundant interfaces on every signal line provide added reliability. Several plating options are available to meet the needs of various applications. The housing material is liquid crystal polymer, compatible with infrared and forced air convection operations. The connector system maintains 50-ohm impedance and uses the solid ground bus between the rows of signals to provide low cross talk and excellent high-speed signal characteristics.

As mentioned previously, AMP part number 767039-1 was the connector used for input, while AMP part number 767089-1 was the connector used for output. Both of these connectors are 38 pin connectors. 767039-1 is a right-angle plug. Figure 74 shows the schematic.

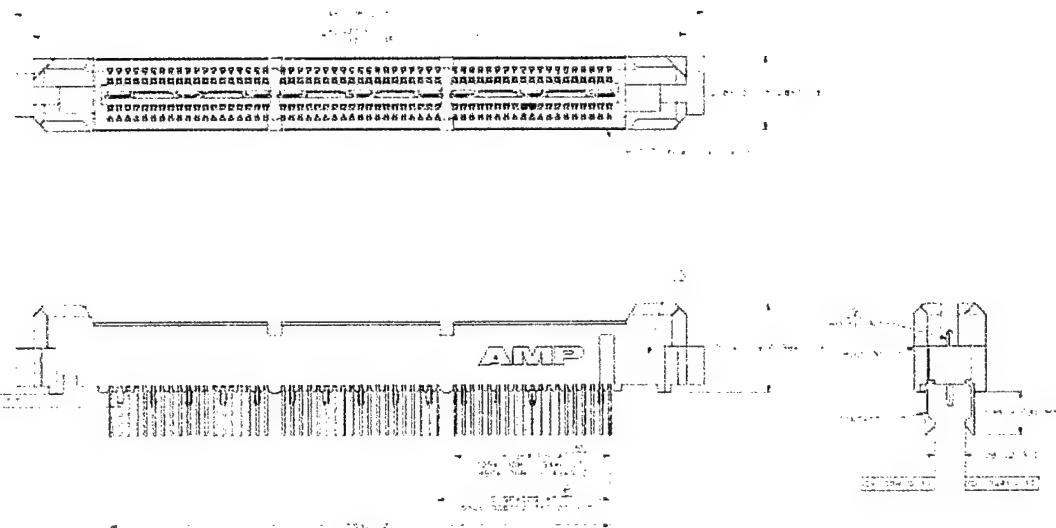


Figure 75. AMP 767039-1 Schematic

767089-1 is a right-angle receptacle. Both of these connectors require the PCB board thickness to be 2.36 mm (0.93 inches). Figure 76 shows the schematic for 767089-1 receptacle.

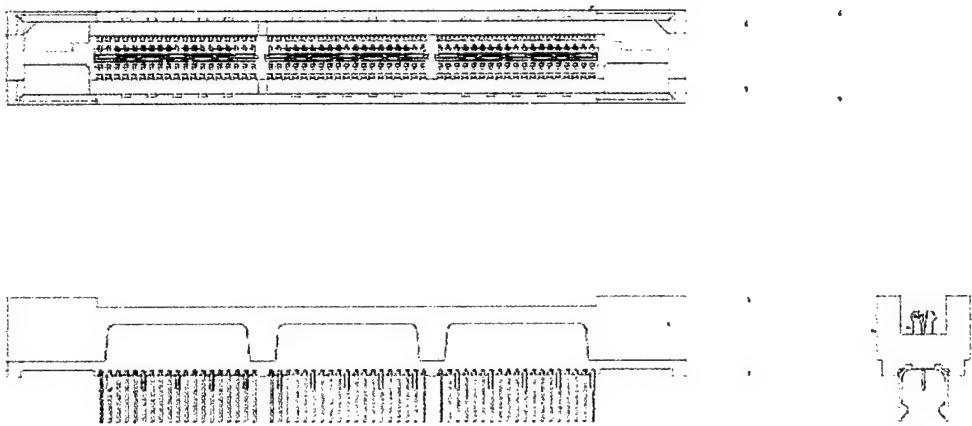


Figure 76. AMP 767089-1 Schematic

6.5.4 Eight Channel Receiver Modular Design

A novel concept was considered for the design of eight-channel receiver, after some consideration. This concept greatly simplified the design and also reduced the size of the board. According to this concept, two different boards were designed, the first board (called daughter board) just consisted of one channel of receiver; while the second board (called motherboard) consisted of the Amp Mictor connectors and the power supply connectors. The daughter boards consisted of leads for inputs, outputs, ground and power supply, which can be connected to the pads on the motherboard. The motherboard

consists of pads to which the leads from daughter boards connect. So to make the eight-channel receiver, eight different daughter boards were mounted on the motherboard. Also, four daughter boards were mounted on the top and four daughter boards were mounted on the bottom. This greatly reduced the size of the motherboard compared with the design shown in Figure 72. Also, each of the daughter board is similar in design to the single channel receiver, which was tested and known to be working. The daughter board is as shown in the Figure 77 below.

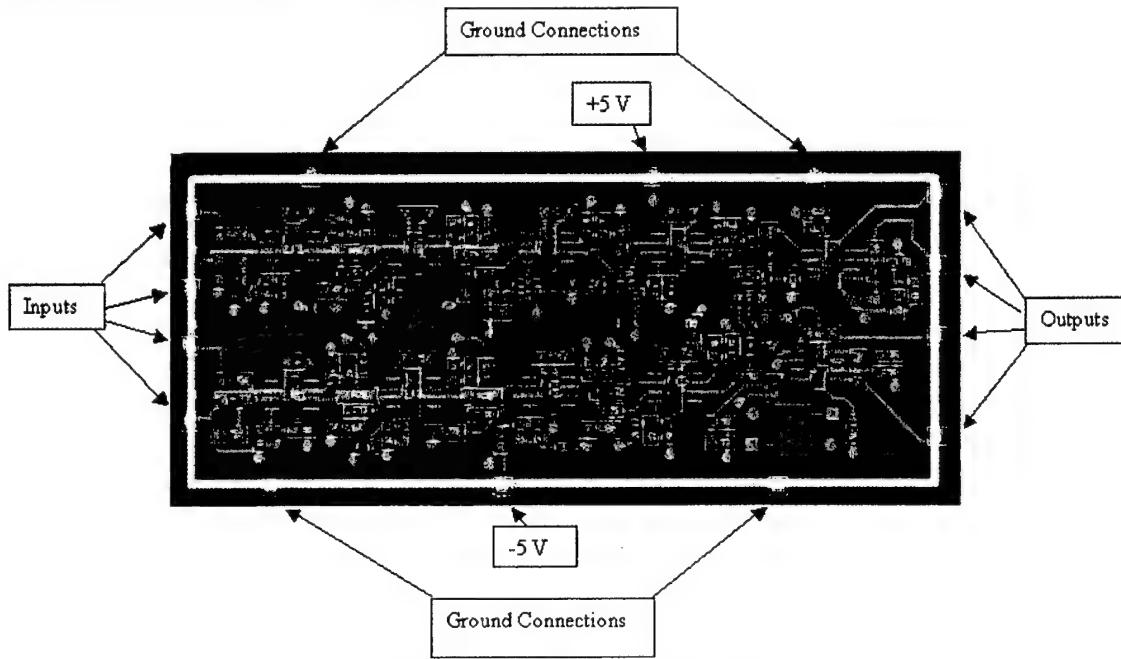


Figure 77. Daughter Board

As can be seen in the figure the daughter board consists of leads all over its edge. These leads connect to the inputs, outputs, ground and power supply on the motherboard. The daughter board is similar in design to the one channel PCB. The specifications for the daughter board are as shown below.

Layers: 4

TOP: Signal

BOTTOM: Signal

POWER PLANE: +5 volts, -5 volts

GROUND PLANE: Analog Ground

The design of the ground plane and the power plane for the daughter board is the same as that of one channel PCB discussed in section 3.3.2 and 3.3.1 respectively. The bottom layer of the daughter board does not have any components or tracks; only the top layer has components and tracks on it.

Figure 78 shows the motherboard.

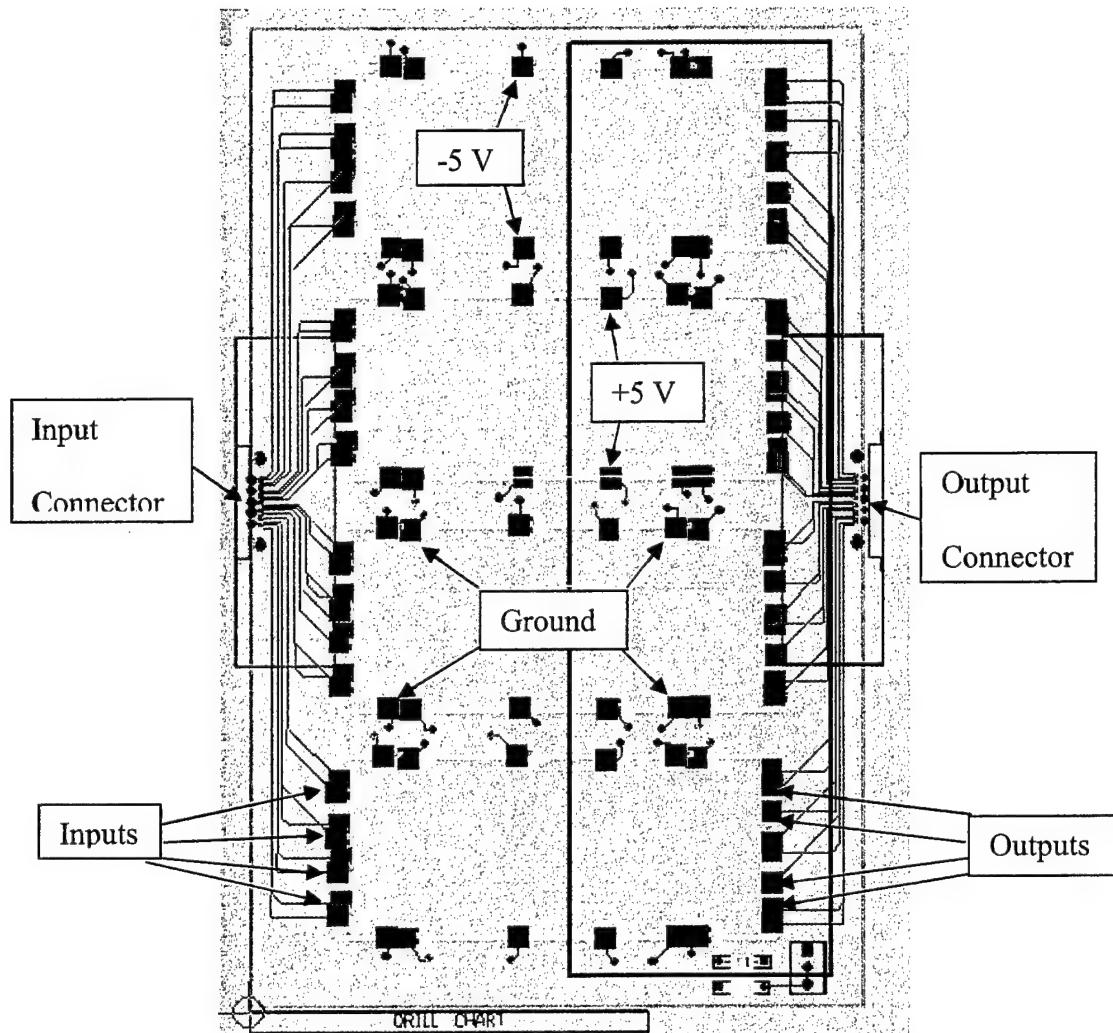


Figure 78. Motherboard

Motherboard also consists of four layers that can be described as below.

Layers: 4

TOP: Signal

BOTTOM: Signal

POWER PLANE: +5 volts, -5 volts

GROUND PLANE: Analog Ground

As shown Figure 78, the motherboards consist of pads, for connecting with the daughter boards. The layout of these pads is exactly same as that of the daughter boards. Both the top and the bottom layer have pads, components and tracks on it. In fact, in this case the bottom layer is the mirror image of the top layer.

The power plane is as shown in Figure 79. The outside rectangle in Figure 78 signifies the outline of the board. The area enclosed by inside rectangle is +5 Volts, while everything else is -5 Volts. This can be seen on the motherboard in Figure 76 too. The entire ground plane for the motherboard is kept undivided, as all daughter boards also have ground plane of their own. The next chapter talks about results and the system

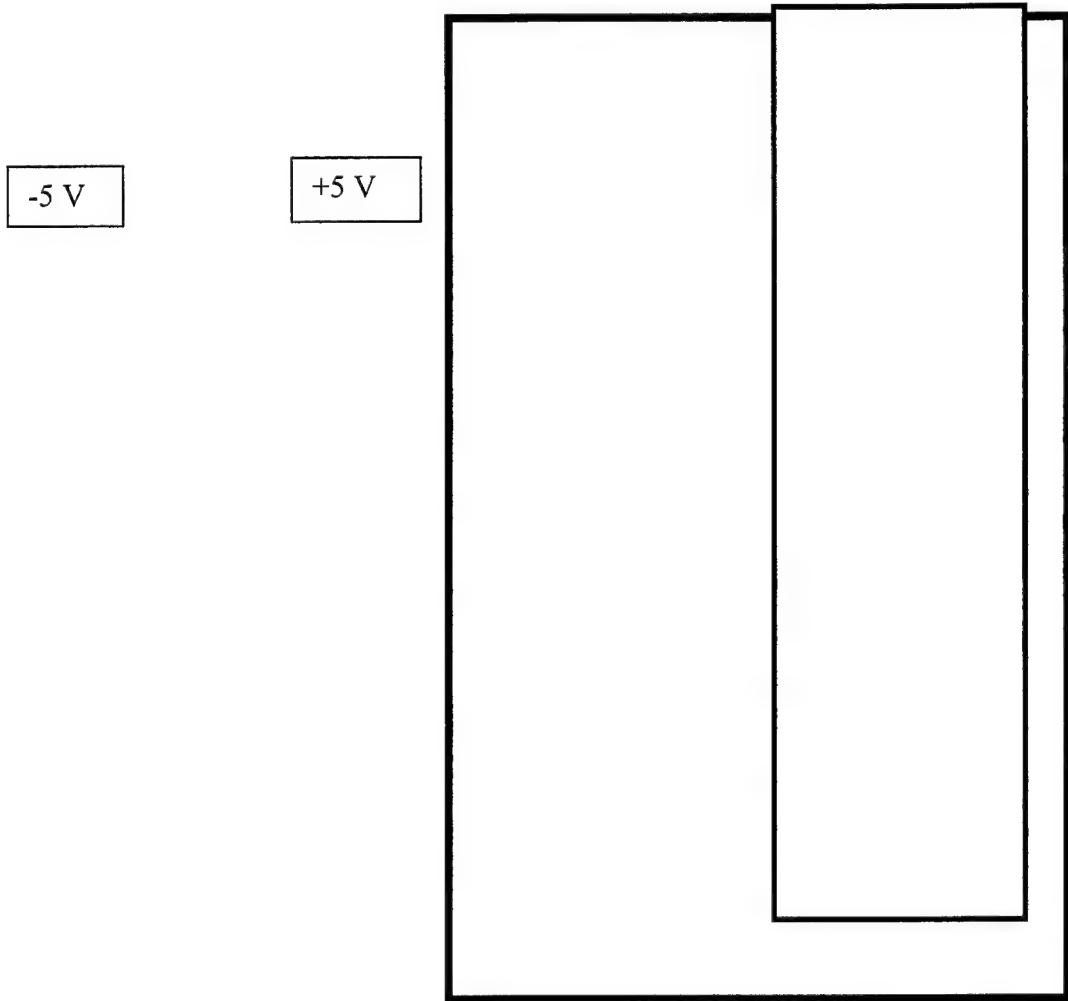


Figure 79: Power Plane for the Motherboard

As can be seen from Figure 80, when both the inputs of the differential amplifier are feed with the same input (100 mV or 1000 mV), the output is almost 0 V. Also, when both the inputs of the difference amplifier are feed with different inputs (0 and 100 mV), the differential amplifier gives an output of around 500 mV, with the gain of 5. This is how the differential amplifier was expected to perform. Thus the differential amplifier functions properly independently.

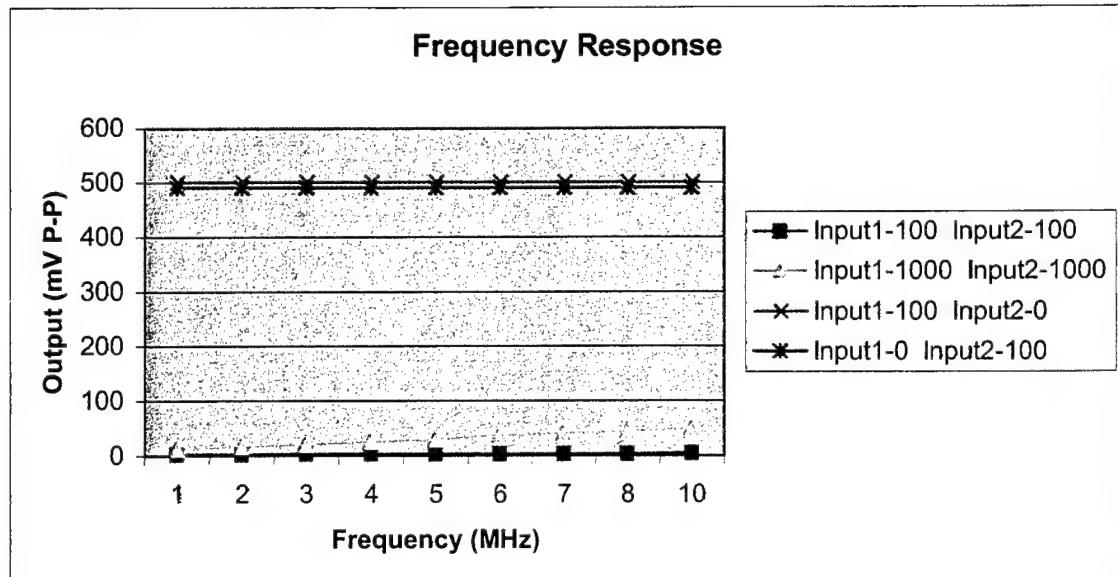


Figure 80. Differential Amplifier Frequency Response

7.0 DESIGN DOCUMENT FOR THE GENERIC BEAMFORMER CARD REQUIREMENTS

7.1 Interfaces

7.1.1 Analog Channel Inputs

The GBF shall receive 18 analog channels. Single ended 50 ohm coax, with a maximum peak to peak voltage level of +/- 140 mv. The mechanical connection shall be an AMP 38 position MICTOR end launch connector. (Part # 7670044-1).

7.1.2 Clock & Trigger Input

The GBF shall receive LVDS level clock and trigger signals. The Trigger signal is 1 clock period in duration and indicates start of transmit cycle. The signals shall be received over 2 pair of coaxes in the same cable as Analog Channel Inputs

7.1.3 Partial Sum Input

The GBF shall receive input of partial sum from adjacent GBF card. Data is two 16 bit data paths. For the ID Beamformer, each path is the same. For the HT Beamformer, the paths are the sine and cosine channels. The input bus shall be functionally and electrically compatible with the FPDP specification, except it shall be designed to operate at 50 MHz synchronous clock rates, and routed over the backplane connector

7.1.4 Partial Sum Output

Output input of partial sum from to GBF card. Data is two 16 bit data paths. ID Beamformer, each path is the same. For HT Beamformer, the paths are the sine and cosine channels. The output bus shall be functionally and electrically compatible with the

FPDP specification, except it shall be designed to operate at 50 MHz synchronous clock rates , and routed over the backplane connector.

7.1.5 Control Interface

Configuration, control and status of the of the GBF shall be performed over the bi-control interface. The control interface shall consist of the following signal shown in Table VIII.

Table VIII: Control Interface Signal

Signal Name	I/O	Description
CDATA[15:0]	I/O	Bi-directional data
CADDR[21:0]	I	On-Board Address
CSEL[4:0]	I	Card Select
CAD[4:0]	I	Card address (Backplane Jumpered)
CRD/WR	I	Read/Write Select
CRST	I	Board Reset
CIRQ	O	Interrupt Request (Open Collector)

This interface shall be used to configure the FPGAs, load the EPROM data tables, configure the operational parameters, read status and transfer data to/from the data collection memories for diagnostic purposes.

7.2 Processing Functions

7.2.1 TVG

The GBF shall provide Time Varying Gain on each of the analog input channels. A common gain curve shall be applied to all 18 channels. The Gain curve shall be downloadable and consist of 64 data values, corresponding to 64 equal range segments. The TVG shall be capable of providing gain from +5 dB to +44 dB in 0.2 dB increments.

7.2.2 Digitization

The GBF shall digitize each of the analog channels with 10 bits of precision.

7.2.3 Buffer Memory

The GBF shall contain sufficient buffer memory to store, at a minimum, 64K 10 bit samples from each of the 18 channels.

7.2.4 Post Trigger Delay

The GBF shall support a programmable post trigger delay. The GBF shall delay data storage from receipt of the trigger signal. The delay shall be programmable from 0 msec to 5 msec with a minimum resolution of 120 usec.

7.3 Signal Processing

7.3.1 Interpolate/Decimate Processing

The GBF shall form beams by providing a variable delay of the data in the 18 channels and then summing these 18 channels together. This sum stream shall be added to the Input Partial sum stream and the result rounded and passed to subsequent GBF for further processing. Time delays shall programmable per beam to within 1/16 th of a sample. The GBF shall support pseudo-dynamic focusing, by providing for adjustable, independent delays on a per-channel basis. The delays shall be updated no faster than once every 41 usec. The delays shall be defined by the user and downloaded onto the GBF and stored in EEPROM.

7.4 Power Control

The GBF shall provide self-power management to reduce overall power consumption. There shall be two power management cycles, *Receive* and *Process*.

During the Receive cycle, the analog circuitry and minimal digital circuitry required to collect the data in the memory shall be enabled. This cycle begins upon receipt of the Xmit Trigger and continues until the required number of samples have been collected.

The Process cycle begins once the Receive cycle is completed. During this cycle, power in the analog circuitry shall be reduced to a minimum and power in the digital circuitry shall be as required.

Power management may be implemented by circuit enables, discrete supply control, and/or clock enables as appropriate.

7.4.1 Power Generation

The GBF shall receive +/- 7v DC power that it will convert to its on-board power requirements as follows:

+5v Analog	0.7 A
-5v Analog	0.4 A
+3v Analog	1.0 A
+3v Digital	0.5 A
2.5v Digital	3.0 A

7.5 Parameter Storage

The GBF shall have the capability to store the interpolation coefficients, TVG tables, and dynamic focusing tables in on-board non-volatile memory.

7.6 FPGA Configuration

The GBF shall support two types of FPGA configuration.

Type 1 is configuration from Control Bus.

Type 2 is configuration from non-volatile memory that was previously loaded over the control interface.

Additionally, the GBF shall support FPGA configuration via the XILINX programming cable for use during initial card test.

The GBF has a 1 Mword configuration memory space as defined in Table IX. All accesses are 16 bit words.

Table IX: GBF Configuration Memory

Address	# Words	Access	Description
	512k	R/W	Buffer Ram Access
	64	R/W	TVG Table #0
	1	R/W	Trigger Delay
	1	R/W	Beam Select
	1	R/W	Mode
	1	R/W	Buffer Memory Bank Select
	8	R/W	FPGA Direct Configuration Registers
	8	R/W	FPGA EPROM Configuration Registers
	8	R/W	Delay EPROM Configuration Registers
	1	W	IRQ Enable Bits
	1	R	IRQ Status Bits
	512	R/W	FPGA Dual Port Access
			Unused

7.7 Buffer Ram Access

This address space allows direct reading and writing of the buffer ram. The RAMS are organized as 3 banks of 32 bits. Each bank will contain 6 channels of A/D data, with 2 bits left over. The 6 channels are organized as two time interleaved channels, three channels wide is shown in Figure 81.

Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bank 0	X	X																														
Bank 1	X	X																														
Bank 2	X	X																														

Figure 81. Buffer Ram Organization

During acquisition, the data is interleaved with the even channels in even 32 bit address and the odd channels at odd 32 bit address.

7.8 Trigger Delay

The Trigger delay is a 16 bit value that specifies the number of clock cycles from receipt of the trigger signal to delay until data collection begins.

7.9 Starting & Ending Beam Select

This 16 bit parameter is used to define the set of beams to process. The Lower byte defines the starting beam number (1-192) and the upper byte defines the ending beam number (1-192).

7.10 TVG Select

This 8 bit parameter is used to select which TVG table to use. A value of 0 specifies the Ram based TVG

7.11 Ram Based TVG table

This 64 byte table defines the 0th TVG table to apply during digitization. This value MUST be downloaded prior to selecting the function

7.12 Mode Register

The GBF can operate in one of three modes Test Mode 1, Test Mode 2 and Process. In addition the Mode register contains the Run/Halt bit that enables the mode.

Test Mode 1: Acquire data after trigger and store in memory, indicate when complete.

Test Mode 2: Process data previously stored in memory.

Process: Continuous processing of data, Acquire and form beams.

7.13 Status Register

The status register contains bits that indicate operational status of the GBF.

7.14 Parameter EPROM

The Parameter EPROM contains the delay tables, TVG tables and Interpolator coefficients for the GBF. This EPROM is programmable over the configuration interface and uses a byte serial programming method, where only the lower 8 bits of the configuration interface are used.

7.15 Memory Map

7.15.1 Delay Tables

The delay tables contain the starting addresses, integer delay values and fractional delay values (in 1/16 sample increments) for each channel. There are 64 sets of delays, corresponding to 64 equal range bins for each channel, and 3 major sets of tables, corresponding to the three operational ranges (1-3, 2-4 and 3-5 meters) . Each delay value consists of 1 byte of integer delay and 1 byte for the fractional delay. These delay tables occupy($(64 * 18 + 1) * 192 * 3$) 1,328,256 bytes of memory. The data is ordered as follows:

7.15.2 TVG Tables

The EPROM contains 8 sets of TVG tables. Each set consists of 64, 8 bit gain values and 1 fixed gain value. The 64 values correspond to the 64 range bins equally spaced across the operational range. The 8 sets allow for 8 different environmental conditions.

7.15.3 Interpolator Coefficients

The EPROM contains the default set of interpolator coefficients used on the GBF.

The FPGA Configuration memory consists of a 16 Mbit EPROM containing up to 3 different FPGA configurations. The 4 bytes of the EPROM contains the starting configuration address that will be loaded into the FPGA upon a card reset.

8.0 THROUGHPUT ANALYSIS OF THE CONVENTIONAL BEAMFORMER

This section presents the analysis of the throughput processing for the diver held sonar. It address three components of the system, the Horizontal Beamformer (HBF), the FFT and the Transfer interfaces to the image processing hardware. It derives the throughput in frames per second for each component and 4 different processing types are used.

1. Beamformer operates at 50 MHz Max.
2. STFT operates at 80MHz max, 512 point FFT with 50% overlap.
3. There are two FFT cards performing the STFT.
4. The Vertical (doily) direction only requires 104 FFT bins to achieve required coverage.
5. The digitized data set consists of 32K of time series data for each element.

8.1 Projection 1: X vs Z

This projection calculates the magnitude of each of the 192 beams along the Z axis. The image is averaged in the Z direction, 128 samples per pixel. No Y axis information is present, no FFT is performed (see Figure 82).

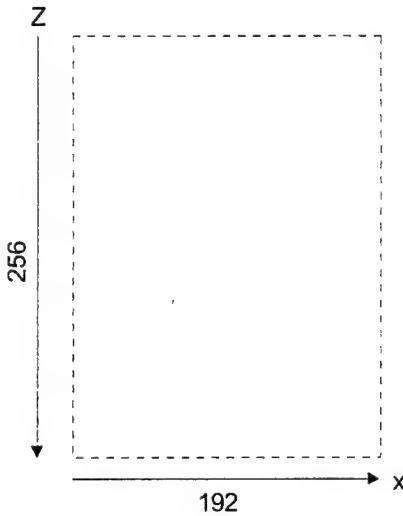


Figure 82. X vs. Z Projection

HBF : 655.4 usec/beam \rightarrow 7.95 FPS for 192 beams

FFT: n/a

8.1.1 Raw Frame Size: 12 Mbytes

Z Averaged Frame Size: 96 kBytes

8.2 Projection 2: X vs Y

This projection computes a 32K FFT for each of the 192 beams. No Z axis information is present. Image data is averaged in the Y direction, 128 FFT bins / pixel, yielding a raw image size of 256 x 192.

HBF: 655.4 usec/beam \rightarrow 7.95 FPS

FFT: 614.4 usec/beam \rightarrow 8.48 FPS

Raw Frame Size: 12 Mbytes

Averaged Y Frame Size: 96 kBytes

8.3 Projection 3: Y vs Z

This projection forms a single sum beam in the horizontal direction and then computes the STFT of the single beam.

HBF: 655.4 usec/beam \rightarrow 1525 FPS for 1 beams

FFT: 819.2 usec/beam \rightarrow 1220 FPS for 1 beams

Frame Size: 26 kBytes

8.4 3D Data

This processing type generates the STFT for all 192 beams (see Figure 83).

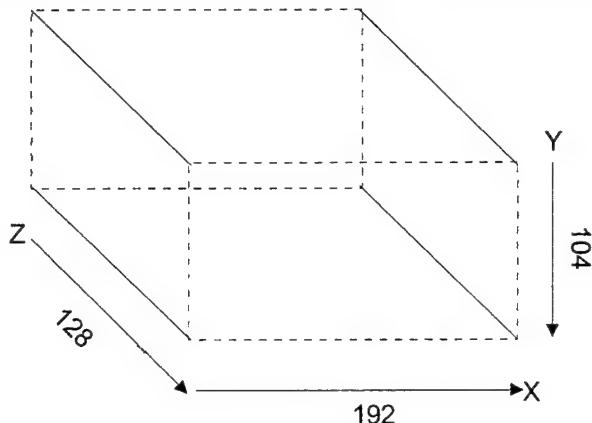


Figure 83. 3D Projection

HBF: 655.4 usec/beam \rightarrow 7.95 FPS for 192 beams

FFT: 819.2 usec/beam \rightarrow 6.35 FPS for 192 beams

Raw Frame Size: 9.75 Mbytes

8.5 Digital Grab Port (DGP)

This is the interface on the Matrox Cards. It is specified at 160 mbytes/sec.

8.6 PCI Bus

Assuming we could get our data to the PCI bus, we could transfer it at 132 mbytes/sec.

The maximum frame rate achievable, based only on the interface transfer rates and the frame sizes is shown in Table X.

Table X: Frame Rates for Projection Options

	DGP	PCI
Projection 1	12.7 FPS	10.4 FPS
Projection 2	12.7 FPS	10.4 FPS
Projection 3	1220 FPS	1007 FPS
3D	6.35 FPS	5.2 FPS

8.7 Conclusions

If we exclude projection 3, it can be seen that the processing rates are between 6.3 FPS and 8.5 FPS. These rates are theoretically all met by the DGP interface and except for case 3D, by the PCI. This assumes that the processing hardware/software can keep up with the data stream. So for this system, the processing and transfer rates are fairly well balanced. The next task is to find out if the image processing can meet these rates.

This section defines the hardware and software interface to the DHS Transmitter Card (DTC) .

The DHS transmitter is a dual channel arbitrary waveform synthesizer. It basic components consists of two FIFOs feeding two D/A converters. The FIFOs are loaded from a PC parallel port. When the card receives a trigger, an internal state machine transfers a frame of data from the FIFOs to the D/A converters, generating the required signal.

The PC parallel port is used to load the FIFOs on the DTC. The port is configured in EPP mode. In this mode, data is transferred in full bytes and the PC hardware controls the handshaking. In addition, transfers can be performed to either the address port or the data port. Transfers to the data port toggle the Data Strobe and are used to write the data to the FIFOs. Transfers to the address port toggle the Address Strobe and are used to configure the mode of the DTC.

In order to place the interface into EPP mode, the port must be configured via the PC's BIOS setup into ECP mode and then configured with software into EPP mode. A complete explanation of these modes may be found at <http://www.senet.com.au/~cpeacock/index.html#PARALLEL>

The transmitter card responds to both data and address strobes from the parallel port. Transfers to the address port will set the "Mode" of the DTC. The mode controls the operation of the transmitter and defines how transfers to the data port shall be interpreted.

9.0 DTC MODES

All mode transfers are a single byte written to the address port on the EPP Parallel port. The DTC recognizes 4 different modes.

9.1 RESET Mode, 0xFF

The DTC is placed into reset mode by writing a 0xFF to the address port. This initializes the DTC and should be performed at the start of a mission.

9.2 Receive Arbitrary Waveform, 0x80

This mode prepares the DTC to receive the arbitrary waveform data and must written to the address port prior to sending data to the card.

9.3 Enable DTC, 0x00

This mode places the DTC into a running state. In this state it will respond to the external triggers and generate the previously loaded data.

9.4 Flush FIFOs, 0x81

This mode clears the data previously stored in the FIFOs. This mode should be asserted prior to reloading the FIFOs with a new arbitrary waveform.

9.5 Arbitrary Waveform Data

Once the DTC is placed into Receive Arbitrary Waveform mode, the data written to the EPP data port is transferred to the FIFOs. The data consists of 32 bit words. Each word contains the 2 channels of sample data and tag bits. The data that is written to the DTC may contain multiple frames of signal data. The DTC will output each frame of data upon receipt of a trigger signal. After the last sample of the last frame is output, the DTC will place the FIFOs into retransmit mode, and begin outputting data from the 1st frame upon receipt of the next trigger signal.

10.0 FIELDS

10.1 CH 1 Data, CH 2 Data

Bits 0-9 defines the 10 bit integer data sample for channel 1 and bits 16-25 define the integer data sample for channel 2.

Table XI. CH1 and CH2 Data Fields

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Byte 1								Byte 0							
1	0	EO F	EO D	0	0	CH 1 Data									

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Byte 3								Byte 2							
0	0	0	0	0	0	CH 2 Data									

10.2 EOD

Bit 12 is the end of data bit. This bit marks the last sample of the last frame of data in the FIFOs. If this bit is set, the EOF bit must also be set.

10.3 EOF

Bit 13 is the end of frame bit. This marks the last sample a frame of data in the FIFOs.

11.0 MATLAB FUNCTION INTERFACE

Specifications for the MATLAB interface should be as follows,

Algorithm: The waveform functions will be computed in double precision floating point. The floats will be converted to 10 bit integer format and stored in a 2D array that has the dimensions of (NFRAMES, NSAMPLES). This 2D array will be downloaded to the FIFO's on the board

12.0 IMAGE PROCESSING HARDWARE FOR THE DIVER HELD SONAR

This paper section the data throughput requirements and a hardware configuration for the image processing function of the Diver Held Sonar. It establishes the input data rates and presents the interface options available assuming the Matrox Genesis image processing boards

12.1 Hardware Configuration

Image processing hardware consists of the Matrox Geniuses image processors fed by the FFT cards and driving a 640x480 TFT LCD display.

12.2 Matrox Genisis Boards

The Matrox boards consist of a Main Board, processor boards and interface daughter cards. The Main board is a full size PCI card that contains 1 processing node and a VGA display controller. This board can be used a the sole VGA controller in a PC system. The processing boards are also full size PCI cards and contain 1 or 2 processing nodes. Up to 5 processor boards and 1 main board may be configured in a system.

12.3 Data Interfaces

In addition to the PCI interface, the Matrox boards each have a Grab port Interface and a VESA Media Channel interface. (VMC)

The VMC interface is a VESA standard and will support a 133 Mbytes/sec digital data stream. This interface in normally used for Matrox board to board data transfers.

The Grab Port Interface is a Matrox proprietary interface and will support up to 200 Mbytes/sec data transfer rates. This is interface is highly configurable and can be used to receive the data from the FFT.

12.4 Video Processing

The Main Processor board has a Video Display Processor that is compatible with Windows 95/NT. This Processor has a dedicated overlay buffer that can be controlled by the processing node on the card. With this arrangement, the ultrasound image can be displayed in real-time along with the standard windows desktop.

12.5 FFT Processors

The FFT processor cards extract the vertical beams by performing a short time Fourier transform on the horizontally formed beams. In essence, each FFT Bin represents a pixel in the vertical direction. These cards can provide the Matrox Cards with 16 bit magnitude-squared data values. If we assume a 512 complex point FFT with a 50% overlap, a 12 MHz sampling rate ,a range gate period of 2.6 ms, and 192 beams then the amount of data produced per frame would, at maximum, be 5.6M samples. If we assume 10 Frames/sec and 16 bit samples, the output of the FFT processing would have an aggregate data rate of around 118 Mbytes/sec, within the maximum bandwidth of the DGP port on the Matrox cards.

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